VOLTAGE REGULATION IN A SINGLE-STAGE THREE-PHASE BOOST-INVERTER USING MODIFIED PHASOR PULSE WIDTH MODULATION METHOD FOR STAND-ALONE APPLICATIONS

by

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B.S, Sharif University of Technology, 2011

A THESIS

submitted in partial fulfillment of the requirements for the degree

MASTER OF SCIENCE

Department of Electrical and Computer Engineering
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KANSAS STATE UNIVERSITY
Manhattan, Kansas

2013

Approved by:

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Abstract

In this thesis, a modified version of the phasor pulse width modulation (PPWM) switching method for use in a single-stage three-phase boost inverter is presented. Because of the required narrow pulses in the PPWM method and limitations in controller resolution, e.g. dSPACE, the desired switching pattern for a boost inverter requires a costly processor. A low resolution processor can cause pulse dropping which results in some asymmetric conditions in output waveforms of the boost inverter and therefore, an increase in the THD of the output waveform. In order to solve this problem, a new switching pattern is developed which guarantees symmetric conditions in the switching pattern by discretizing the switching pattern in every switching cycle. This switching pattern has been applied to a boost inverter model developed by SimPowerSystems toolbox of MATLAB/Simulink. The model has been simulated in a wide range of input DC voltage and load. Moreover, a laboratory-scaled three-phase boost inverter has been designed, built, and tested using an identical switching pattern in the same input voltage and load range. Both simulation and experimental results confirm the effectiveness of the new switching pattern.

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Acknowledgements

I would like to express my gratitude to my supervisor, Dr. Behrooz Mirafzal for useful comments, remarks, and engagement throughout the learning process of this master thesis. Besides my advisor, I would like to thank Dr. Anil Pahwa and Dr. Ruth Douglas Miller for serving on my committee, as well as support along the way. Also, I would like to thank Ms. Akanksha Singh for her help in running some tests in the laboratory.

Dedication

I would like to dedicate my thesis to my family for nursing me with affection and love and their dedicated partnership for success in my life. A special feeling of gratitude to my loving parents and sister whose words of encouragement and push for tenacity always rings in my ears.

Chapter 1 - Introduction

1.1 Motivation

Nowadays, renewable or sustainable energy resources, such as photovoltaic panels and wind turbines play an important role in the electric power generation system. Connecting these energy resources (which are part of distributed resources) to the power grid will help reduce dependency of the electric grid on the price and availability of fossil fuels such as oil and coal. It will also reduce emission of greenhouse gases from fossil-based power generation units. Another advantage of these resources over centralized power plants is the fact that they can be located near loads and, therefore, they do not necessarily need bulky transmission and distribution systems. While in a power system, cost of transmission and distribution system is approximately equal to 30% of the total cost of the system, use of distributed resources will reduce the total cost of the system [1]. One of the most important types of renewable energy resources is photovoltaic (PV) resources. Worldwide annual solar PV energy capacity between 1995 and 2012 is shown in Figure 1.1 [2]. Increase in efficiency and reduction of cost of PV systems has dramatically increased the tendency to use this energy resource. It is believed that by 2040, this type of energy resource will become the most prominent supplier of electrical energy among all of the renewable energy resources [3]. However, one concern in regards to

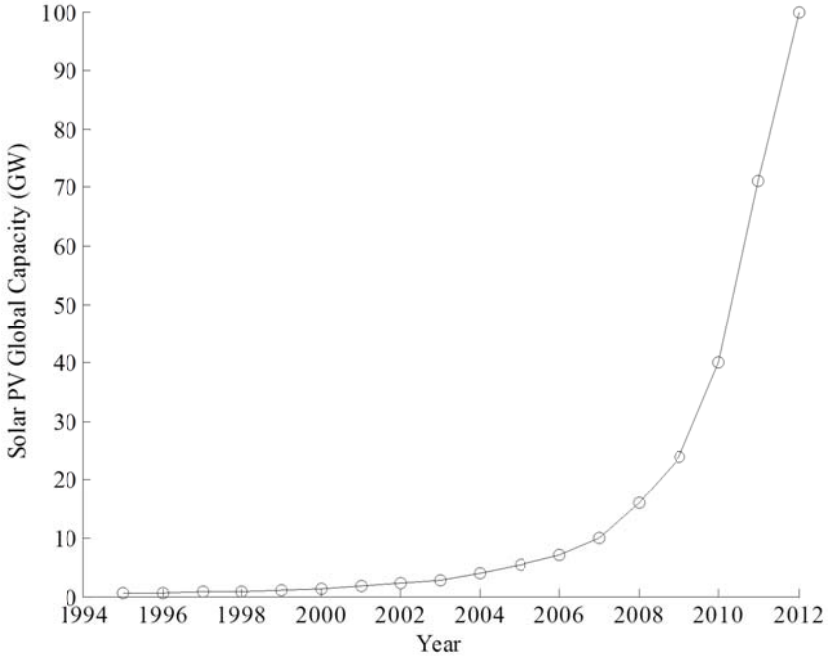


Figure 1-1 Solar PV Global Capacity

the use of these resources is that the energy produced is in a form that cannot be directly connected to the power grid. Therefore, power electronic interface circuits are required to convert output of these resources to a form that is compatible with the power grid or can be used by local load. The output signal waveform of renewable energy resources is either DC (solar panels) or AC (wind turbines). While the magnitude of DC and AC waveforms and frequency of AC waveforms are changing based on environmental conditions such as irradiation level of sunlight and wind speed, a DC/DC converter and control strategy is used to convert the output signal of these resources to a constant DC signal. In the next level, a DC/AC inverter should be connected to the system to produce a sinusoidal waveform that can be used in either stand-alone or grid-connected applications. The DC voltage that PV systems can produce is usually lower than the required value to generate peak voltage (in stand-alone applications) or peak grid voltage (in grid-connected applications). Therefore, in addition to changing the input DC voltage to AC voltage with a constant magnitude and frequency, the interface circuit should also be able to boost voltage to the required level. An alternative method is to use several PV panels in series to increase the input DC voltage, which would cancel the need to boost the input voltage. However, this will decrease the reliability of the system, because if one of the panels fails or there is shadowing on one of the panels, the performance of the system will not be ideal anymore. Moreover, using a boost inverter would increase the robustness of the system, because there is an inductor in the DC link of the inverter which would limit inverter output currents in case of short-circuit faults in the system.

1.2 Background

Previously, some studies have been conducted on the application of using current source inverters as a boost inverter for renewable energy systems [4, 5, 6, 7]. In [4], a transformerless three-phase current-source inverter has been presented which provides an output voltage of several hundred volts when its input is connected to a PV module. Also, in [5], the concept of one cycle control (OCC) has been used with a current source inverter for grid-connected single-stage boost inverters. In [6], the necessity of “shoot through” state has been emphasized by using Tri-Level PWM Logic instead of Bi-Level PWM Logic in order to boost input DC voltage to a required peak to peak AC voltage.

In [7], Phasor Pulse Width Modulation (PPWM) which is derived based on the concept of Space Vector Pulse Width Modulation (SVPWM), has been introduced and it has been applied to a three-phase single-stage boost inverter. In this method, at each instance, two switches are 'ON' (one switch from the top row (S_{ap}, S_{bp}, S_{cp}) and one switch from the bottom row (S_{an}, S_{bn}, S_{cn}) to make a path for the current of DC link inductor). Every switching cycle is divided into three time intervals (states), one charging state, and two discharging states. During the charging state, both of the switches in a leg of the inverter are 'ON', and during each discharging state, one switch from the top row and one switch from the bottom row that are not in the same leg are 'ON', simultaneously. In this method, the duration of discharging intervals has been found using the fact that integration of voltage of DC link inductor over each switching cycle is zero and duration of charging interval has been found by subtracting these discharging times from switching cycle period. A sinusoidal waveform at the output of the boost inverter can be obtained by applying these charging and discharging times on the inverter switching pattern.

1.3 Problem Statement

Limitations in controller resolution (e.g. dSPACE) cause some pulse dropping in the generated switching pattern of phasor pulse width modulation method. This pulse dropping results in some asymmetric conditions in output voltage and current waveforms of the boost inverter and therefore, THD of the output waveform increases. In order to solve this problem, a new approach for the aforementioned PPWM switching pattern is developed herein to avoid this pulse dropping and guarantee symmetric conditions in the switching pattern.

Moreover, in the DC link of the boost inverter, an inductor with a high inductance value is necessary, in order for the inverter to be able to boost the input DC voltage to an AC voltage with a desired amplitude. While this inductor is relatively large, integrating it with other circuit components into a single package would help reduce the total size of the circuit.

The objectives of this work are to achieve the required THD of the single-stage three-phase inverter output waveforms and integrate its DC link inductor to PV panels.

1.4 Thesis Outline

Besides this introductory chapter, this thesis includes seven additional chapters and four appendices. In Chapter 2, several interface circuits that can be used to connect PV panels to local load or electrical grid are discussed. In Chapter 3, an overview of pulse width modulation

(PWM) and different PWM methods are introduced, then, space vector pulse width modulation (SVPWM), which is one of the most popular PWM methods, is briefly explained. In Chapter 4, integration of PV panels with DC link inductor of three-phase boost inverter is investigated with a goal of reducing total size of the circuit. In Chapter 5, PPWM is discussed in detail, then, the technical concerns of implementing the PPWM method are mentioned and a modified PPWM is proposed. In Chapter 6, Simulink model of the boost inverter is developed (complete Simulink model is available in Appendix B), the modified PPWM method is applied to this model and the results for several input DC voltage and loads are shown. Also, the results of applying the same method to the system with higher resolution are presented. Moreover, a comparison between the results of applying PPWM and modified PPWM is given. In Chapter 7, modified PPWM method is applied to a laboratory-scale three-phase boost inverter (PCB design layout and information of the boost inverter are available in appendix A. Also snubber and gate drive circuits are available in Appendix C). Experimental results verify the developed switching pattern (A table including all of the simulation and experimental results is presented in Appendix D). In Chapter 8, conclusion of this thesis and suggested future work are given.

Chapter 2 - Interface Circuits for Photovoltaic Systems

2.1 Introduction

As it was mentioned in previous chapter, power electronic interface circuits are required to convert output of renewable energy resources to a form that is compatible with the power grid or can be used by the local load.

In the design of these interface circuits, several challenges and issues must be taken into consideration. Some of these issues are:

1) Power Density: One factor that should be considered in the design of every circuit is to make it as compact as possible. Currently, power density goal for inverter circuits is approximately 1 W/cm^3 [3].
2) Efficiency: The ratio of inverter output power to its input power is defined as the efficiency of that inverter. The design goal of every inverter is to maximize the efficiency. However, a trade-off always exists between inverter performance and cost. The efficiency of the inverters connected to photovoltaic systems is typically lower than efficiency of bulky inverters [8].
3) Reliability: It is important that lifetime of interface circuits used to connect PV panels to electrical grid/local load be approximately equal to the life of PV panels. Typically, PV panel life is more than 20 years [9] meaning that ideally, inverters should be able to work for this length of time. However, studies have shown that the primary reason of failure in PV systems is due to the failures in the inverters [10]. Reliability can be measured using two factors [3]:
    a) Mean time between failures (MTBF): The mean time between failures is typically ten years for inverters.
    b) Mean time to first failure (MTFF): The mean time to first failure is typically five years for inverters.
4) Balance of system cost: Balance of system (BOS) is defined as the total PV system cost except the cost of the PV panel itself. System cost can reduce by decreasing the cost of the components used in the interface circuits as much as possible [3].

Several interface circuits can be designed with consideration of these four issues. In this chapter, a brief explanation of some of the circuits is given.

This chapter contains eight sections. In each section, a special type of interface circuit between the PV module and electrical grid/local load is presented and discussed. In Section 2.2, voltage source inverter is used as the interface circuit and problems associated with using this inverter as the interface circuit are discussed. In Section 2.3, the interface circuit includes a transformer and two options for use of the transformer are presented. In the first case, a DC/AC inverter is in series with a line frequency transformer and in the second case, an inverter, high frequency transformer, and AC/AC inverter are connected in series. In Section 2.4, the interface circuit consists of a DC/DC boost converter in series with a voltage source inverter. The DC/DC converter is used to reduce the input needed to achieve peak desired output voltage. However, using two circuits in series makes the interface system more complex. In Sections 2.5 and 2.6, use of a multilevel inverter and a Z-source inverter as the interface circuit is presented, respectively and some of the advantages and disadvantages of each case is discussed. In Section 2.7, a single-stage boost inverter is presented as an interface circuit. In this work, for the single-stage three-phase boost inverter, a new switching pattern will be introduced. Finally, in the last section, a conclusion of the chapter is given.

2.2 Interface Circuit using a Voltage Source Inverter

One simple way to connect PV panels to the electrical grid/local load is to connect the panels in series and then connect them to a voltage source inverter (VSI). Figure 2-1 shows a three-phase conventional voltage source inverter.

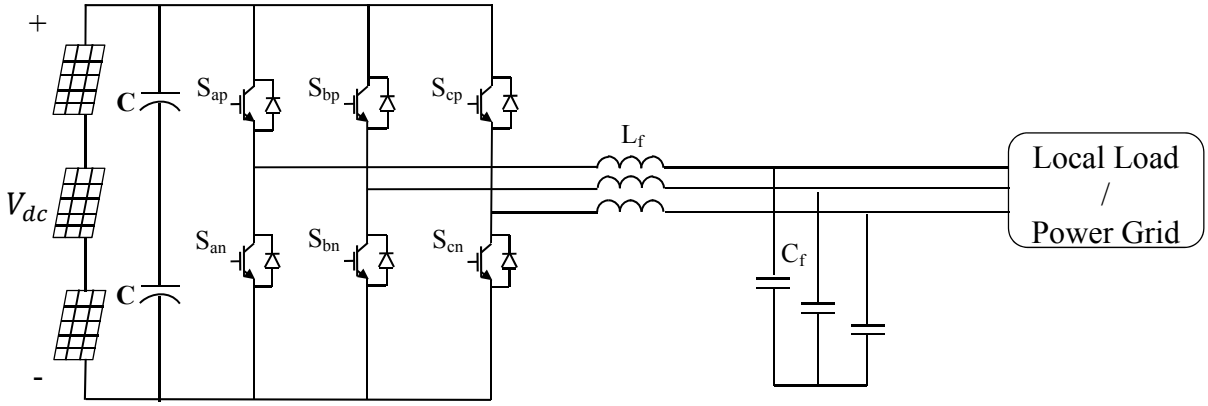


Figure 2-1 Schematic of a Three Phase Conventional Voltage Source Inverter

In this figure, the group of series PV panels has been shown as a voltage source. The voltage

source inverter, consisting of six switches and filter, is used to convert the DC input signal into a sinusoidal waveform which can be fed to a local load/electric grid. Each switch consists of a power transistor and an anti-parallel diode, which provide a two directional path for current.

Although this method may seem inexpensive and simple, various problems are associated with it. One of the biggest problems of this method is its lack of reliability. While the voltage source inverter works as a buck inverter, its input voltage should be more than desired peak output voltage, therefore, a number of PV panels should be connected in series to increase the input DC voltage. If one of these panels fails, while the panels are in series, the system will not experience ideal performance. Also, if shadowing occurs on one of the panels, the input signal will decrease, leading to less output voltage in the AC side and decreased efficiency of the system. Another disadvantage of voltage source inverters is that two switches in the same leg cannot be 'ON', simultaneously, because a shoot-through will happen and two sides of the input voltage source will be short-circuited which will damage the components in the circuit. This usually happens because of electromagnetic interference (EMI) in the circuit. The shoot-through can be avoided by adding dead time to switch operating time; however, this dead time causes distortions in the output waveform and increases total harmonic distortion (THD).

2.3 Interface Circuit using a Transformer

Another configuration that can connect PV panels to the electrical grid/local load is the use of a transformer. In this method, output voltage of the photovoltaic module is first converted to an AC signal using a DC-AC inverter. In the next stage, output of the inverter is fed to the load through a transformer providing the desired output signal. Two types of transformers that can be used in this case:

1) Line Frequency Transformer
2) High Frequency Transformer

Figure 2-2 shows the interface circuit using a line frequency transformer. In this case, the DC-AC inverter converts input DC voltage into a sinusoidal waveform with a frequency of 60Hz (line frequency). Then, the line frequency transformer is used to boost voltage amplitude to the desired value.

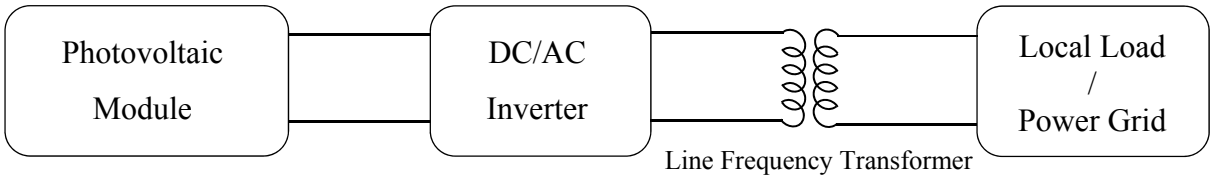


Figure 2-2 Boost Using a Line Frequency Transformer

Based on Faraday's law of induction, magnetic flux induces a voltage which is in the opposite direction of the main voltage. This voltage is equal to:

$$v = N\frac{d\varphi}{dt} \quad (2.1)$$

By assuming that the input voltage is sinusoidal, magnetic flux in the core will also be a sinusoidal signal. Therefore if it is assumed that

$$\varphi = \varphi_m * \sin(\omega t) \quad (2.2)$$

Where φ_m is the maximum value of the magnetic flux and ω is the angular frequency of the waveform, the result from using equations (2.1) and (2.2) is

$$v = N * \varphi_m * \omega * \cos(\omega t) \quad (2.3)$$

Root mean square (rms) value of the above signal is equal to:

$$vrms = \frac{N * \varphi m * \omega}{\sqrt{2}} \quad (2.4)$$

By using "$\varphi m = A * Bm$" in equation (2.4), the result will be:

$$v_{rms} = 4.44 * f * N * A * B_m \quad (2.5)$$

The disadvantage of using a line frequency transformer is that, while its frequency is low, based on equation 2.5, it is very bulky and expensive. Therefore, to reduce the circuit size, high frequency transformers are being used. Figure 2-3 depicts the interface circuit using a high frequency transformer. In this case, the input from the photovoltaic module is converted to a sinusoidal waveform with a high frequency. Then, the high frequency transformer is used to boost the voltage level to the desired value, and, finally, the AC-AC inverter converts the sinusoidal waveform frequency to the line frequency (60Hz) [11].

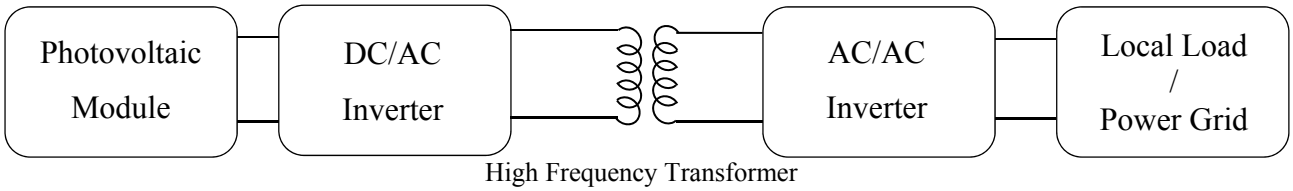


Figure 2-3 Boost Using a High Frequency Transformer

2.4 Interface Circuit using a DC-DC Converter in Series with a Voltage Source Inverter

Figure 2-4 shows a two stage circuit topology that can be used to boost input DC voltage to a desired AC signal. In this circuit, the DC-DC converter is used as a maximum power point tracker (MPPT) to regulate input voltage from photovoltaic modules. It is also used to amplify input voltage (by using a DC-DC boost converter) and in the next stage, the inverter is used to generate AC voltage.

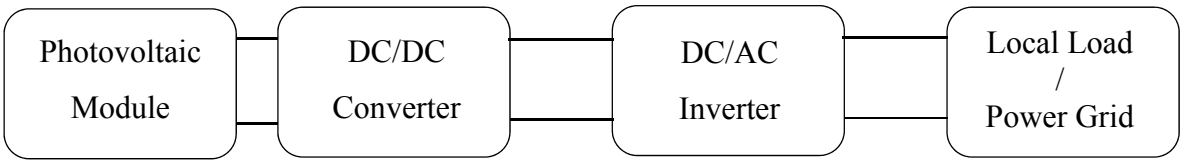


Figure 2-4 Boost Using a DC-DC Converter and a DC-AC Inverter

Various drawbacks are associated with using the previously described topology. First of all, each conversion stage in the circuit needs a separate control system, thus making the total system control scheme more complicated than previous options. Secondly, as shown in Figure 2-5, the DC-DC converter stage (assumed to be a boost converter) in the above circuit has a solid state switch and an electrolytic capacitor which will make the circuit less reliable and less efficient [12].

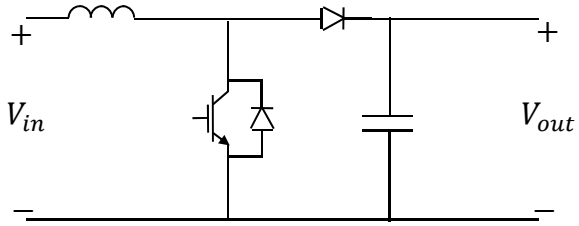


Figure 2-5 DC-DC Boost Converter

2.5 Interface Circuit using a Multilevel Inverter

Multilevel inverters are another option that can be connected between photovoltaic panels and local load/power grid. Multilevel inverters consist of power switches, diodes, and capacitors working as voltage sources for the circuit. The output signal of multilevel inverters is a stepped waveform which can be filtered to achieve a sinusoidal waveform as the output of the interface circuit. Some primary advantages of using multilevel inverters are [13]:

1) Distortion in the output voltage signal and $\frac{dv}{dt}$ is very low in these inverters.

2) These inverters can operate using lower switching frequencies.
3) Smaller filter can be used to provide an acceptable sinusoidal waveform out of the output signal of the inverter, therefore reducing the total cost of the system.

However, aside from noted advantages, various disadvantages are also associated with this interface, too. Increased complexity of the inverter control system is one of the difficulties of using these inverters. Also, because of the increase in the number of components used in the circuit, the reliability of the system lessens and its cost increases [14].

2.6 Interface Circuit using a Z-Source Inverter

Impedance source or Z-source inverter is another option that can connect photovoltaic modules to the local load/power grid. Z-source inverters can boost and invert in one stage using fewer solid state switches than conventional boost inverter circuits. Figure 2-6 shows the general structure of a Z-source inverter. Switches used in the inverter block can either be a power transistor in parallel with an anti-parallel diode (as shown in Figure 2-7) or a power transistor in series with a power diode (as shown in Figure 2-8). Typically, a diode is connected in series with the input source to prevent reverse current flow. The advantage of using a Z-source inverter is that it can be used as a Buck-Boost inverter, meaning that amplitude of the output signal can be less or more than the input voltage. However, a disadvantage of using the Z-source inverter is that its input current has high ripples that put stress on the inductor and capacitor located in the DC side of the circuit [15], [16].

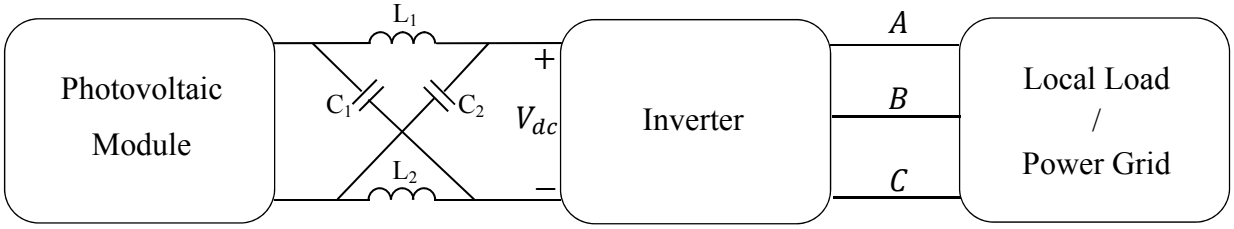


Figure 2-6 General Structure of the Z-source Inverter

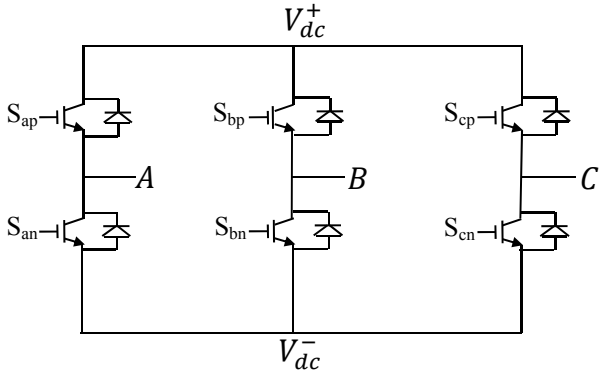


Figure 2-7 Inverter Block of Figure 2.6 Using a Power Switch and an Anti-Parallel Diode

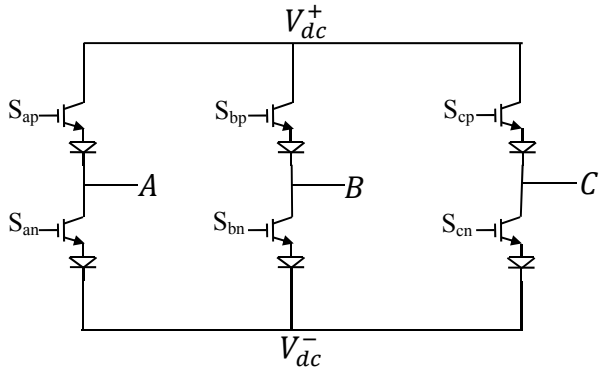


Figure 2-8 Inverter Block of Figure 2.6 Using a Power Switch with a Diode in Series

2.7 Interface Circuit using a Single–Stage Boost Inverter

The final interface circuit discussed in this chapter and majority of this thesis discussions will be based on it is a boost inverter. By using this inverter with a special type of switching pattern (to be discussed later) and an appropriate control strategy, boosting and inverting input DC voltage into a sinusoidal waveform in one stage can be achieved. The circuit configuration of a boost inverter has been shown in Figure 2-9. A detailed explanation of circuit performance, switching pattern, and control strategy used to obtain the desired output signal will be provided in the following chapters.

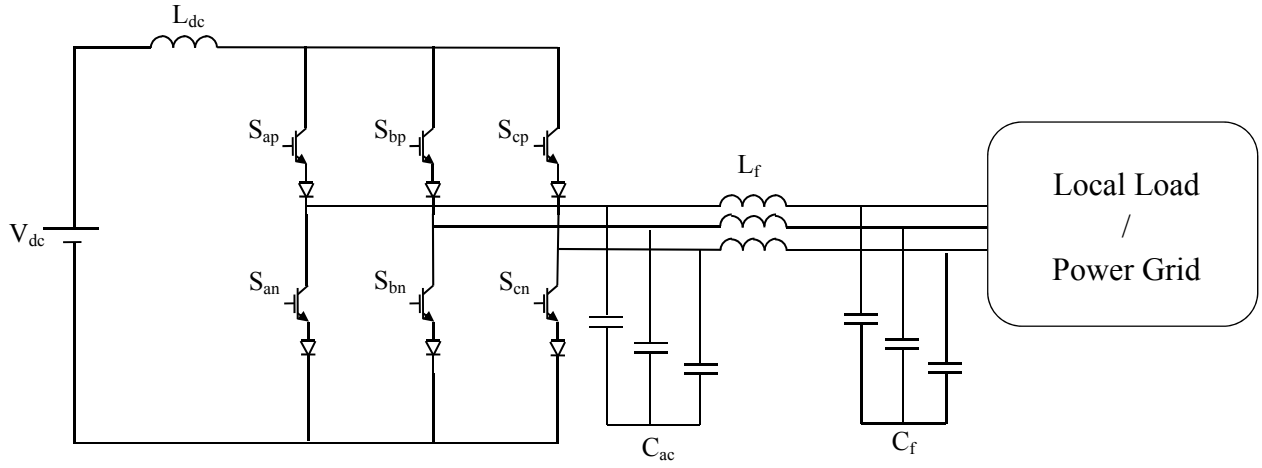


Figure 2-9 Circuit Configuration of a Single-Stage Three-Phase Boost-Inverter

2.8 Conclusion

In this chapter, various interface circuits that can be connected between the photovoltaic panels and the electric grid/local load are presented and for each circuit, the advantage and disadvantages of using these circuits are mentioned. These interface circuits are necessary because the input voltage source, assumed to be a photovoltaic panel, generates a DC voltage and a sinusoidal waveform is desired in the output (electric grid/local load). Therefore,

an interface circuit should convert the input DC signal to an AC signal. In Chapter 4, some investigation on reduction of the boost inverter size would be done and then, performance of this inverter will be investigated using a special pulse width modulation switching technique and an appropriate control strategy.

Chapter 3 - Overview of Pulse Width Modulation (PWM)

3.1 Introduction

Pulse Width Modulation (PWM) is one of the most popular switching strategies used to control output voltage of inverters. This method is based on changing the duty cycle of inverter switches in order to reduce harmonics in the output waveform of the inverter. Although a lot of research has been conducted in developing several types of PWM techniques, the basics of PWM is to compare a reference waveform and a carrier waveform (usually a sawtooth or triangular waveform) and set the duty cycle of the switches based on this comparison.

In this chapter, a brief introduction to different types of PWM will be given. In Section 3.2, a brief introduction of pulse width modulation and its fundamentals is given and, in its following sections, different methods of modulation are discussed. In Section 3.3, naturally sampled pulse width modulation is introduced. This method has been discussed using two types of carrier waveform. In Subsection 3.3.1, a sawtooth carrier waveform is used and in Subsection 3.3.2, a triangle carrier waveform is used. In Section 3.4, regular sampled pulse width modulation is defined. This method is studied in more detail in Subsections 3.4.1 and 3.4.2 using sawtooth and triangle carrier waveforms. In Section 3.5, space vector pulse width modulation (SVPWM) is described and in Section 3.6, its relationship to sampled PWM is discussed. In the last section, a conclusion of chapter is given.

3.2 Pulse Width Modulation Fundamentals

In general, the concept of pulse width modulation method is to compare a high frequency carrier waveform with a low frequency reference waveform and use the comparison results to determine ‘ON’ and ‘OFF’ times of the switch. Therefore, the first objective is to find the ‘ON’ and ‘OFF’ times of each switch in order to achieve these pulses. Based on this information, the final result of all modulation methods is a train of pulses. The problem associated with these trains of pulses is that they contain higher harmonics as well as the main harmonic. Therefore, second goal of every PWM strategy is to minimize these unwanted harmonic distortions. Minimizing these unwanted harmonics from the output waveform will also reduce the losses in the system.

The most popular method of finding harmonic components of a PWM signal has been

developed by Bowes and Bird [17].

In this method, two time variable signals are defined as:

$$x(t) = \omega_c t + \Theta_c \quad (3.1)$$

$$y(t) = \omega_o t + \Theta_o \quad (3.2)$$

Where $\omega_c = \frac{2\pi}{T_c}$ and $\omega_o = \frac{2\pi}{T_o}$ are the carrier and reference angular frequency, T_c and T_o are the carrier and reference signal period interval and Θ_c and Θ_o are phase angle of carrier and reference signals, respectively.

A function can be defined as $f(t) = f(x(t), y(t))$ where the value of the function can be assumed to be the output voltage of an inverter leg. While both $x(t)$ and $y(t)$ are periodic, value of $f(t)$ is constant for cyclic variations of $x(t)$ and $y(t)$. Also, if both the carrier and reference waveform frequencies are scaled to be presented in radians so that they span from $-\pi$ to π, there are some contours within the $[-\pi{:}\pi,-\pi{:}\pi]$ square (unit cell) in which the value of the function $f(t)$ is constant. Figure 3-1 shows contours associated with a sample function within the unit cell.

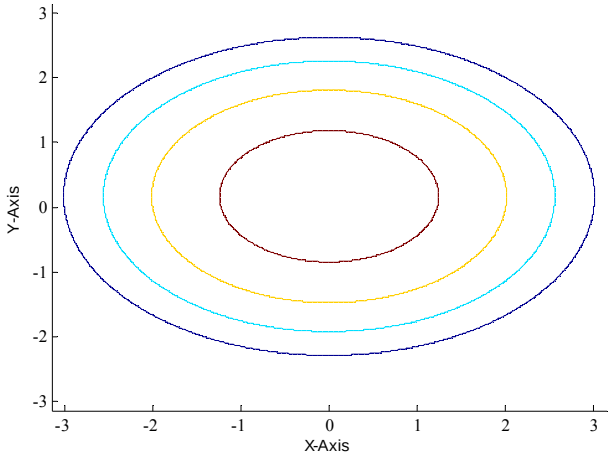


Figure 3-1 Contours of a Sample Function within a Unit Cell

The value of the function $f(t) = f(x(t), y(t))$ at any point in the unit cell can be expressed as a Fourier series. For a two variable function, the Fourier series is defined as:

$$f(x,y) = \frac{A_{00}}{2} + \sum_{n=1}^{\infty}[A_{0n}\cos(ny) + B_{0n}\sin(ny)] + \sum_{m=1}^{\infty}[A_{m0}\cos(mx) + B_{m0}\sin(mx)] + \sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ (n\neq 0)}}^{\infty}[A_{mn}\cos(mx+ny) + B_{mn}\sin(mx+ny)] \quad (3.3)$$

Where

$$A_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} f(x,y)\cos(mx+ny)\,dxdy \quad (3.4)$$

$$B_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} f(x,y)\sin(mx+ny)\,dxdy \quad (3.5)$$

By replacing equations (3.1) and (3.2) into equation (3.3), the result will be:

$$f(x,y) = \frac{A_{00}}{2} + \sum_{n=1}^{\infty}[A_{0n}\cos(n(\omega_o t + \Theta_o)) + B_{0n}\sin(n(\omega_o t + \Theta_o))] + \sum_{m=1}^{\infty}[A_{m0}\cos(m(\omega_c t + \Theta_c)) + B_{m0}\sin(m(\omega_c t + \Theta_c))] + \sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ (n\neq 0)}}^{\infty}[A_{mn}\cos(m(\omega_c t + \Theta_c) + n(\omega_o t + \Theta_o)) + B_{mn}\sin(m(\omega_c t + \Theta_c) + n(\omega_o t + \Theta_o))] \quad (3.6)$$

In the equation above, $\frac{A_{00}}{2}$ is the DC offset component of the PWM waveform, 'm' is the carrier index variable and 'n' is the baseband index variable. Frequency of each harmonic of output voltage can be defined as '$m\omega_c + n\omega_o$'. For example, $m = 1$ and $n = 2$ is the second sideband harmonic in the group of harmonics around the main carrier harmonic.

Generally, the ratio of ω_o and ω_c is not always an integer. Therefore, the pulse train which is the output waveform of one leg of the inverter is not periodic. However, if equations (3.4) and (3.5) are evaluated over many cycles of the reference waveform, eventually, integration of carrier cycles will also be periodic.

Two methods exist to determine the 'ON' time of switches in a power inverter. In the following sections, each PWM method is investigated using one leg of an inverter. These methods are [18]:

1) Naturally Sampled PWM
2) Regular Sampled PWM

3.3 Naturally Sampled Pulse Width Modulation

The most straightforward modulation strategy is naturally sampled pulse width modulation. In this method, a low frequency reference waveform is compared to a high frequency carrier waveform. At any instant, if the reference waveform is greater than the carrier waveform, the output signal is equal to its upper bound and if the reference waveform is less than the carrier waveform, the output signal is equal to its lower bound value. In order to be able to get a sinusoidal output using this method, the reference waveform should be in the form of:

$$v_r = Mcos(\omega_o t + \Theta_o) \tag{3.7}$$

Where M is the modulation index, ω_o is the desired output frequency and Θ_o is the output phase.

Two types of waveforms can be used as the carrier waveform. The carrier waveform can either be a sawtooth or a triangle waveform [18].

3.3.1 Sine-Sawtooth Modulation

Figure 3-2 shows one leg of an inverter in which naturally sampled Sine-Sawtooth modulation is implemented. As mentioned before, this modulation compares a sinusoidal reference waveform to a sawtooth waveform and, based on the comparison, either the top switch (S_{ap}) or the bottom switch (S_{an}) turns on. Therefore, if it is assumed that the value of the function $f(x, y)$ is equal to V_{AN}, only two values for the function can be obtained, $2V_{dc}$ and 0. The unit cell in Figure 3-3 shows values of the function based on variations in the reference and carrier signal.

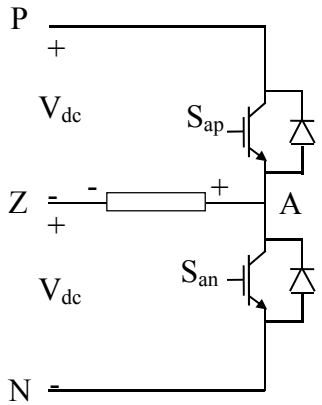


Figure 3-2 One Leg of an Inverter

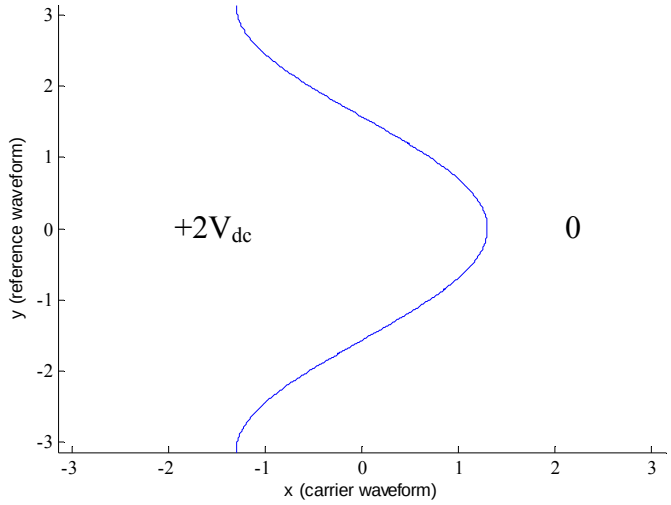


Figure 3-3 Unit Cell for Sine-Sawtooth Naturally Sampled PWM

The boundary between two areas defines intersection points of carrier and reference waveform. If phase angles of both reference and carrier waveforms are zero, for particular values of ω_c and ω_o, these points can be found by intersecting $y = \frac{\omega_o}{\omega_c} x$ line with the boundary locus (It should be noted that while both x and y are periodic in time, the unit cell is replicating in both directions as shown in Figure 3-4).

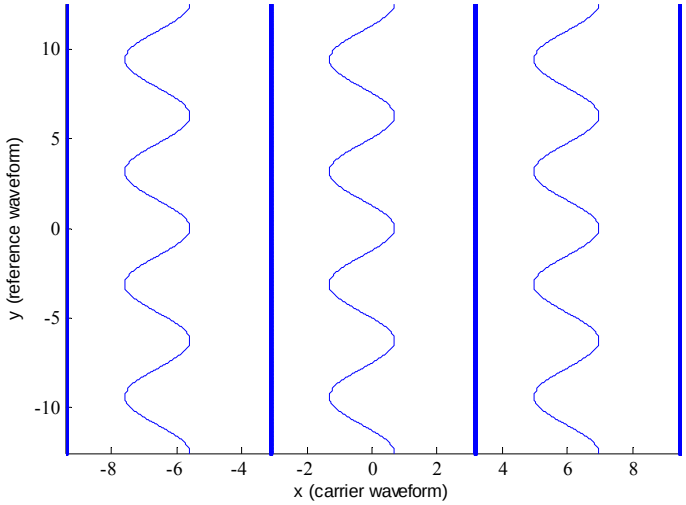


Figure 3-4 Replicated Unit Cells along both X-Axis and Y-Axis

Therefore, $f(x, y)$ changes from 0 to $2 * V_{dc}$ when

$$x = \pi(2 * n - 1) \qquad n = 0,1, \ldots \tag{3.8}$$

And it changes from $2 * V_{dc}$ to 0 when

$$x = 2\pi * n + \pi M cos(\omega_o t) \qquad n = 0,1, \ldots \tag{3.9}$$

Using the x-values above, value of the function $f(x,y)$ can be plotted with respect to the reference waveform as shown in Figure 3-5.

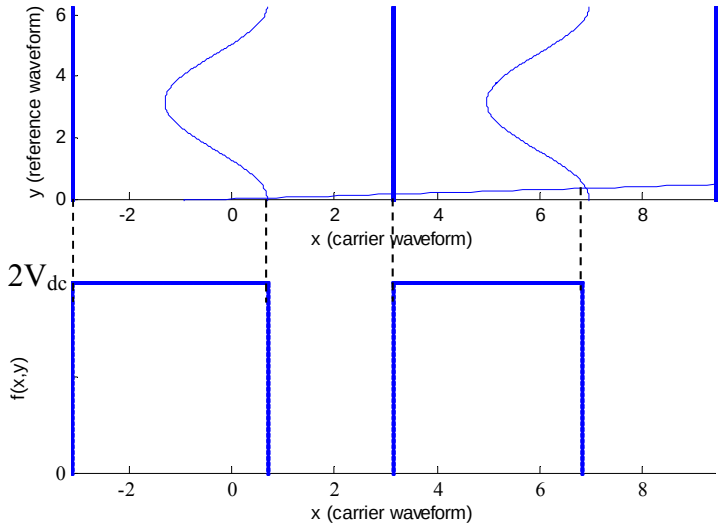


Figure 3-5 a) Three Unit Cells Showing the Relationship between Reference and Carrier Waveform and Their Boundary b) The Value of f(x,y) with respect to the Carrier Waveform in Sine-Sawtooth Modulation

By having the waveform of $f(x,y)$ as shown in Figure 3.5b, coefficients of the Fourier series can be found by using equations (3.4) and (3.5). After finding all coefficients, $f(x,y)$ can be written as a summation of its harmonics using equation (3.6).

3.3.2 Sine-Triangle Modulation

The more common type of naturally sampled PWM is the Sine-Triangle modulation. In this method, a reference sinusoidal waveform is compared to a triangular waveform. If this method is applied to one leg of an inverter, as shown in Figure 3-2, the value of the function $f(x,y)$, which is V_{AN}, can only take two values, $2V_{dc}$ and 0. The unit cell in Figure 3-6 shows values of the function based on variations in the reference and carrier signals.

As in the previous case, the same process can be performed to find the value of the function. In this case, $f(x,y)$ changes from 0 to $2 * V_{dc}$ when

$$x = 2\pi n - \frac{\pi}{2}(1 + M cos\omega_o t) \qquad n = 0,1,\ldots \qquad (3.10)$$

And it changes from $2 * V_{dc}$ to 0 when

$$x = 2\pi n + \frac{\pi}{2}(1 + M cos\omega_o t) \qquad n = 0,1,\ldots \qquad (3.11)$$

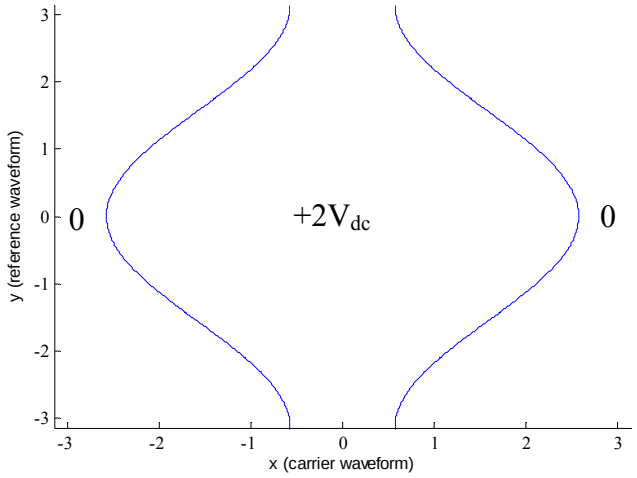


Figure 3-6 Unit Cell for Sine-Triangle Naturally Sampled PWM

Using the x-values above, value of the function $f(x,y)$ can be plotted with respect to the reference waveform as shown in Figure 3-7.

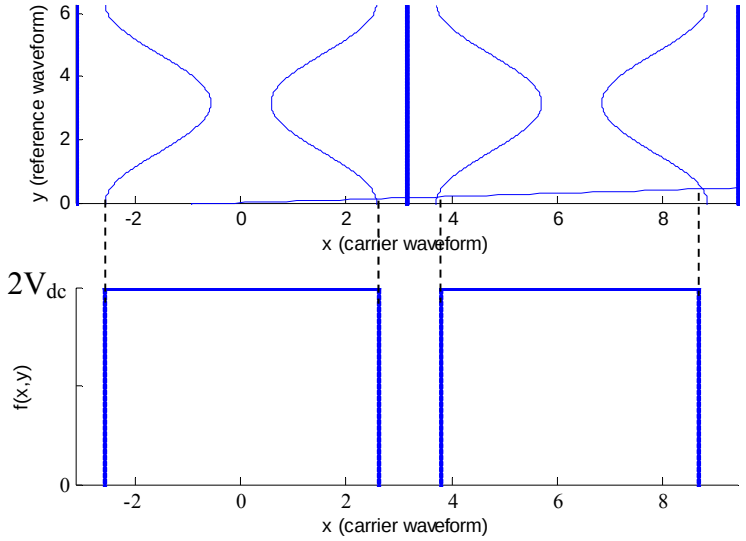


Figure 3-7 a) Three Unit Cells Showing the Relationship between Reference and Carrier Waveform and Their Boundaries b) Value of f(x,y) with respect to the Carrier Waveform in Sine-triangle Modulation

By using equations (3.4) and (3.5), coefficients of the output waveform can be found.

The advantage of using a sinusoidal over a sawtooth reference waveform is that all even baseband harmonics around the even carrier wave harmonics and all odd baseband harmonics around the odd carrier wave harmonics are zero.

3.4 Regular Sampled Pulse Width Modulation

The biggest issue associated with naturally sampled PWM is complexity associated with finding the intersection points between the reference and carrier waveforms is complex. Therefore, an alternative method, called "regular sampled pulse width modulation", can be used. In this method, the reference waveform is sampled and held constant during sample points and then, the new sampled waveform is compared to the carrier waveform. As in naturally sampled PWM, the carrier waveform can either be a sawtooth waveform or a triangle waveform.

3.4.1 Sawtooth Carrier

In this strategy, samples are taken at the intersection of the reference waveform and rising edge of the sawtooth waveform. The value of the sampled function is then held constant until the next sampling point as shown in Figure 3-8.

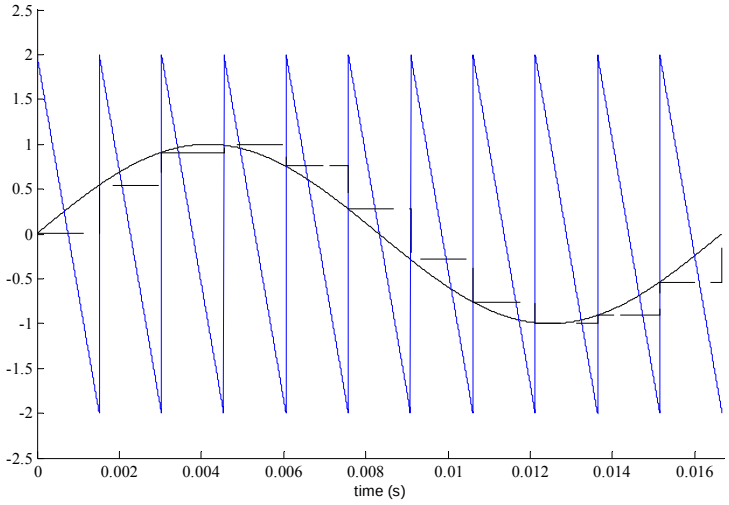


Figure 3-8 Sawtooth Carrier Regular Sampled PWM

If one leg of an inverter, as shown in Figure 3-2 is used and the assumption is made that value of $f(x, y)$ is equal to V_{AN}, based on the figure above, intersection points can be found by crossing the boundary locus and a step function whose value is held constant over each period of the carrier waveform, shown in Figure 3-9 below. (The boundary locus is identical to that shown in Figure 3-4).

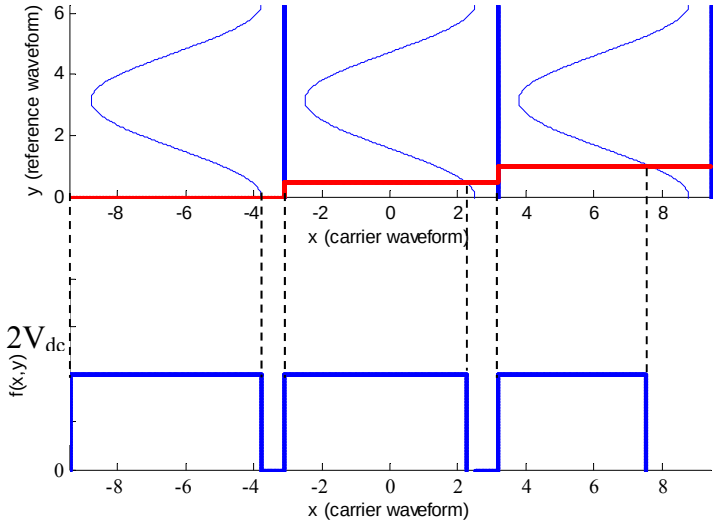


Figure 3-9 a) Three Unit Cells Showing the Relationship between Reference and Carrier Waveform and Their Boundary b) Value of f(x,y) with respect to the Carrier Waveform in Sawtooth Carrier Modulation

Therefore, $f(x,y)$ changes from 0 to $2 * V_{dc}$ when

$$x = \pi(2 * n - 1) \qquad n = 0,1,\ldots \tag{3.12}$$

And it changes from $2 * V_{dc}$ to 0 when

$$x = \pi M cos\left(\frac{\omega_o}{\omega_c} 2\pi n\right) = \pi M cos(y') \qquad n = 0,1,\ldots \tag{3.13}$$

Where:

$$y' = y - \frac{\omega_o}{\omega_c}(x - 2\pi n) \tag{3.14}$$

3.4.2 Symmetrical Regular Sampled PWM

Symmetrical regular sampled PWM can be achieved if the same strategy as Section 3.4.1 is used with a triangular carrier waveform instead of a sawtooth carrier waveform. In this method, the reference waveform is sampled once every carrier period at the positive or negative peak of the carrier waveform and held constant until the next peak (as demonstrated in Figure 3-10). If function $f(x,y)$ is defined as V_{AN} in Figure 3-2, the same method as previously described can be used to find the intersection points as shown in Figure 3-11.

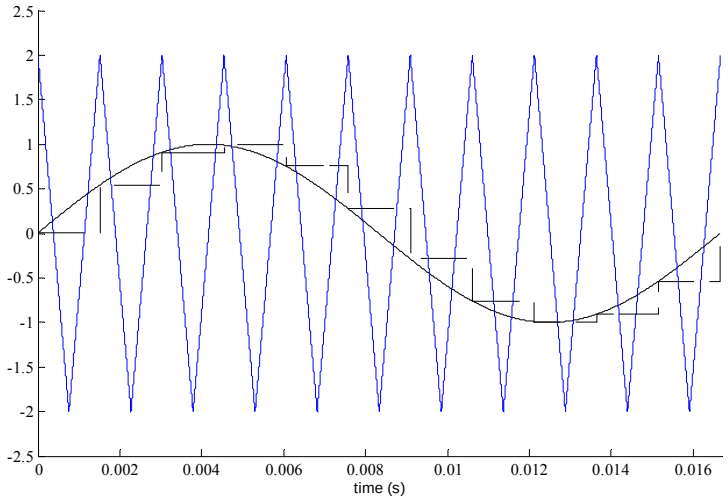


Figure 3-10 Symmetrical Regularly Sampled PWM Sampling Method

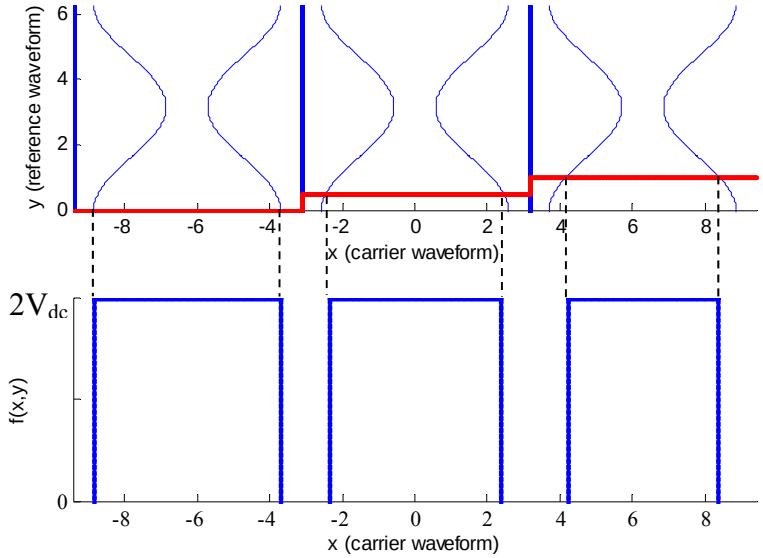


Figure 3-11 a) Three Unit Cells Showing the Relationship between Reference and Carrier Waveform and Their Boundary b) Value of f(x,y) with respect to the Carrier Waveform in Symmetrical Regular Sampled PWM

3.4.3 Asymmetrical Regular Sampled PWM

Compared to symmetrical regular sampled PWM in which the reference is sampled once every carrier interval, in asymmetrical regular sampled PWM, the reference is resampled every half carrier interval at both positive and negative carrier peaks. Therefore, two samples are present in every carrier interval as shown in Figure 3-12.

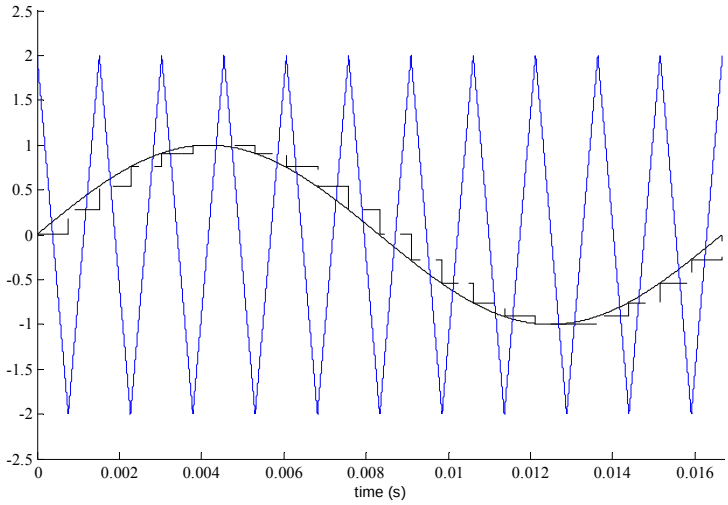


Figure 3-12 Asymmetrical Regularly Sampled PWM Sampling Method

3.5 Space Vector Pulse Width Modulation

One of the most popular types of pulse width modulation methods is space vector pulse width modulation (SVPWM). In order to understand the SVPWM method, six vectors are assumed, as shown in Figure 3-13. Each of these six vectors, which divide the [0,2π] interval into six parts, represents one of the switches of an inverter i.e. voltage source inverter. Half of a circle with a center at the intersection point of these vectors is then assumed. This half circle is rotating counterclockwise with an angular frequency of $2\pi f$ where f is the desired output frequency. At each instance, three of the six vectors fall inside this half circle. Switches associated with vectors inside the half circle at each instance are assumed to be 'ON'. If the angle associated with S_{ap} is assumed to be $\Theta = 0$, Table 3-1 shows the on switches with respect to Θ.

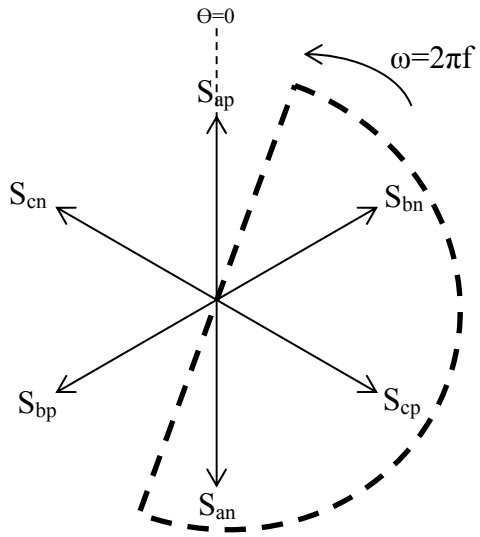


Figure 3-13 Vectors Dividing the Plane into Six Parts

Table 3-1 ON Times of Switches of a Voltage Source Inverter based on Figure 3-13

Sector	Θ	ON Switches
I	$0<\Theta<\frac{\pi}{3}$	S_{ap} , S_{bn} , S_{cp}
II	$\frac{\pi}{3}<\Theta<\frac{2\pi}{3}$	S_{cn} , S_{ap} , S_{bn}
III	$\frac{2\pi}{3}<\Theta<\frac{3\pi}{3}$	S_{bp} , S_{cn} , S_{ap}
IV	$\frac{3\pi}{3}<\Theta<\frac{4\pi}{3}$	S_{an} , S_{bp} , S_{cn}
V	$\frac{4\pi}{3}<\Theta<\frac{5\pi}{3}$	S_{cp} , S_{an} , S_{bp}
VI	$\frac{5\pi}{3}<\Theta<\frac{6\pi}{3}$	S_{bn} , S_{cp} , S_{an}

Based on information in Table 3-1, line to neutral voltages across each phase of the load can be found (load assumed to be in Y configuration). For example, in sector I, S_{ap} , S_{bn} , S_{cp} are ON meaning that the equivalent circuit of the inverter is as shown in Figure 3-14. This information is provided in Table 3-2.

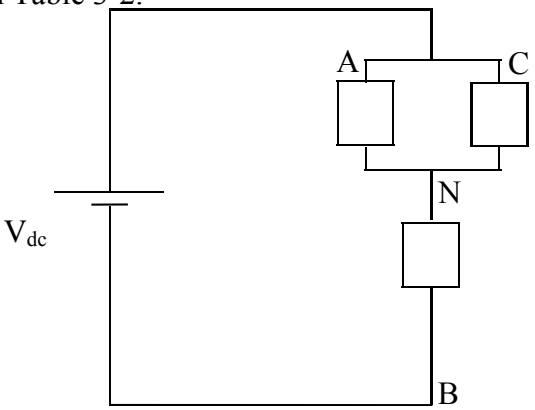


Figure 3-14 Equivalent Circuit of a Three Phase Voltage Source Inverter in Sector I

Table 3-2 Voltage Across each Phase of Load in Different Sectors

Sector	V_{AN}	V_{BN}	V_{CN}
I	$\frac{V_{dc}}{3}$	$\frac{-2V_{dc}}{3}$	$\frac{V_{dc}}{3}$
II	$\frac{2V_{dc}}{3}$	$\frac{-V_{dc}}{3}$	$\frac{-V_{dc}}{3}$
III	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{-2V_{dc}}{3}$
IV	$\frac{-V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$\frac{-V_{dc}}{3}$
V	$\frac{-2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$
VI	$\frac{-V_{dc}}{3}$	$\frac{-V_{dc}}{3}$	$\frac{2V_{dc}}{3}$

Now, a space vector can be defined as shown below.

$$\vec{V}_s = \frac{2}{3}\left(V_{AN} + e^{j\frac{2\pi}{3}}V_{BN} + e^{j\frac{4\pi}{3}}V_{CN}\right) \quad (3.15)$$

Using equation (3.15) for each row of Table 3-2 gives a vector associated with it. These vectors are shown in Table 3-3.

Table 3-3 Space Vector Values in Different Sectors

Sector	V_s
I	$\frac{2}{3}V_{dc}e^{j\frac{5\pi}{3}}$
II	$\frac{2}{3}V_{dc}e^{j0}$
III	$\frac{2}{3}V_{dc}e^{j\frac{\pi}{3}}$
IV	$\frac{2}{3}V_{dc}e^{j\frac{2\pi}{3}}$
V	$\frac{2}{3}V_{dc}e^{j\frac{3\pi}{3}}$
VI	$\frac{2}{3}V_{dc}e^{j\frac{4\pi}{3}}$

As it can be seen in Table 3-3, all space vectors have the same magnitude and each two consecutive space vector are 60 degrees apart. These vectors are shown in Figure 3-15.

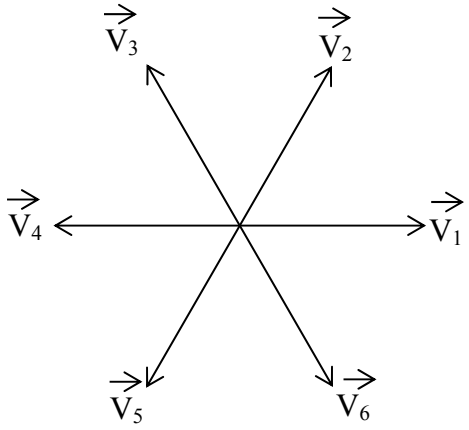


Figure 3-15 Space Vectors for Different Sectors

In general, the goal of every switching strategy is to make the desired output phase voltages to be sinusoidal with identical amplitude and 120 degrees difference. If it is assumed that the phase

voltages are $V_{AN}^{*} = V_m \sin(\omega t)$, $V_{BN}^{*} = V_m \sin\left(\omega t - \frac{2\pi}{3}\right)$ and $V_{CN}^{*} = V_m \sin(\omega t - \frac{4\pi}{3})$, the space vector associated with these three voltages can be found using equation (3.15).

$$\vec{V}_s = \frac{2}{3}\left(V_{AN} + e^{j\frac{2\pi}{3}} V_{BN} + e^{j\frac{4\pi}{3}} V_{CN}\right) = \frac{2}{3}\left(V_m \sin(\omega t) + e^{j\frac{2\pi}{3}} V_m \sin\left(\omega t - \frac{2\pi}{3}\right) + e^{j\frac{4\pi}{3}} V_m \sin\left(\omega t - \frac{4\pi}{3}\right)\right) = V_m e^{j\omega t} \quad (3.16)$$

This vector has a constant amplitude of 'V_m' and is rotating with an angular frequency of 'ω'. Therefore, at each instance, this vector falls into one of the sectors shown in Figure 3-15. In every sector, this vector should be written as a linear combination of the zero vector and two space vectors surrounding that vector. For example, if the desired space vector is between $\vec{V}_1$ and $\vec{V}_2$:

$$\vec{V}_s = d_1\vec{V}_1 + d_2\vec{V}_2 + d_z\vec{V}_z \quad (3.17)$$

Values of 'd_i' above can be found using the following equations which is based on law of Sines.

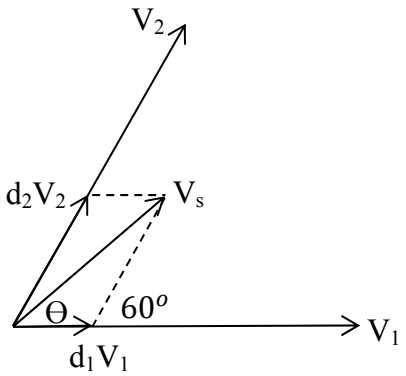


Figure 3-16 Desired Space Vector Shown as a Linear Summation of two Space Vectors

$$\frac{V_m}{\sin(\frac{2\pi}{3})} = \frac{d_1(\frac{2V_{dc}}{3})}{\sin(\frac{\pi}{3} - \Theta)} = \frac{d_2(\frac{2V_{dc}}{3})}{\sin(\Theta)} \Rightarrow d_1 = \frac{\sqrt{3}V_m}{V_{dc}}\sin(\frac{\pi}{3} - \Theta)$$

$$d_2 = \frac{\sqrt{3}V_m}{V_{dc}}\sin(\Theta)$$

$$d_z = 1 - d_1 - d_2 \quad (3.18)$$

'd_1','d_2' and 'd_z' are duty ratios in [0,1] interval and defined as $d_1 = \frac{t_1}{T_s}$, $d_2 = \frac{t_2}{T_s}$ and $d_z = \frac{t_z}{T_s}$ where 't_1' is the time that the system should stay in 'V_1', 't_2' is the time that the system should stay in 'V_2', 't_z' is the time that the system should stay in 'V_z' and 'T_s' is the switching cycle period ($t_1 + t_2 + t_z = T_s$).

3.6 Relationship between Space Vector PWM and Regular Sampled PWM

Although the formulation for space vector PWM is different from the sampling PWM methods previously discussed, they have certain similarities. In this section, the relationship between these two methods will be discussed.

As it was mentioned in previous sections, in the sampling pulse width modulation methods, a high frequency carrier waveform is compared to a low frequency reference waveform and the comparison result determines the state of switches in the system. Figure 3-17 shows a Sine-Triangle modulation for a three-phase system.

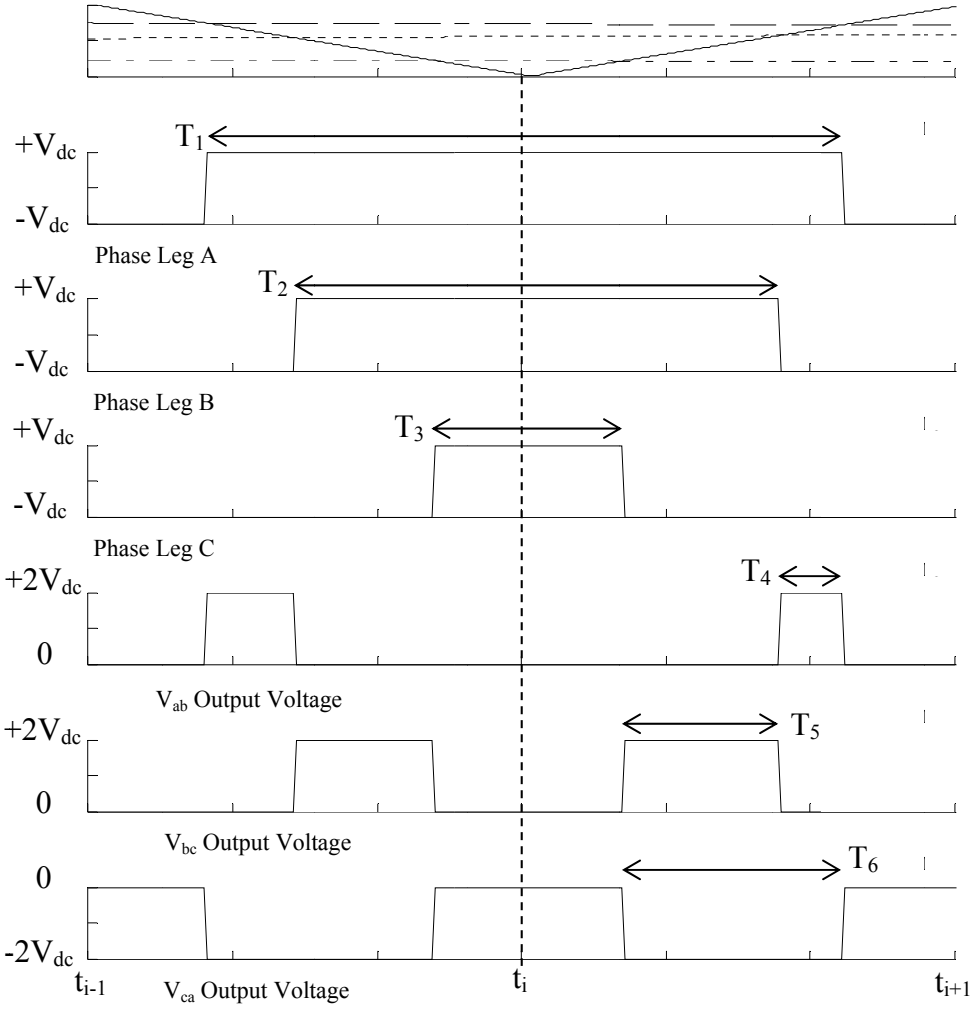


Figure 3-17 Expanded View of a Sine-Triangle Modulation for a Three Phase System over One Carrier Interval

The first plot in Figure 3-17 shows three reference waveforms along with the carrier waveform, the second plot shows the switching pattern for S_{ap} (switching pattern for S_{an} is

logical NOT of S_{ap}), the third plot shows the switching pattern for S_{bp} (switching pattern for S_{bn} is logical NOT of S_{bp}), the fourth plot shows the switching pattern for S_{cp} (switching pattern for S_{cn} is logical NOT of S_{cp}), the fifth plot shows the pattern for the output V_{ab} (derived from subtracting switching pattern of S_{bp} from S_{ap}), the sixth plot shows the pattern for the output V_{bc} (derived from subtracting switching pattern of S_{cp} from S_{bp}) and the seventh plot shows the pattern for the output V_{ca} (derived from subtracting switching pattern of S_{ap} from S_{cp}). The length of each switching pulse can be found using the equations below. In these equations, $T_s = \frac{1}{f_s}$, where f_s is the switching frequency and ω is the desired output angular frequency. Proof of these equations is out of the discussions of this thesis and can be found in pulse width modulation literature.

$$T_1 = \frac{T_s}{2}\left\{1 + Mcos(\frac{\omega(t_i + t_{i+1})}{2})\right\} \tag{3.19}$$

$$T_2 = \frac{T_s}{2}\left\{1 + Mcos(\frac{\omega(t_i + t_{i+1})}{2} - \frac{2\pi}{3})\right\} \tag{3.20}$$

$$T_3 = \frac{T_s}{2}\left\{1 + Mcos(\frac{\omega(t_i + t_{i+1})}{2} + \frac{2\pi}{3})\right\} \tag{3.21}$$

Based on these equations, length of pulses of line to line voltage can be found.

$$T_4 = \frac{T_1 - T_2}{2} = \frac{T_s}{4}\left\{\sqrt{3}Mcos(\frac{\omega(t_i + t_{i+1})}{2} + \frac{\pi}{6})\right\} \tag{3.22}$$

$$T_5 = \frac{T_2 - T_3}{2} = \frac{T_s}{4}\left\{\sqrt{3}Mcos(\frac{\omega(t_i + t_{i+1})}{2} - \frac{\pi}{2})\right\} \tag{3.23}$$

Comparing equations (3.22) and (3.23) with equation (3.18) shows that these two methods result in similar switching time intervals [18].

3.7 Conclusion

In this chapter, various methods for pulse width modulation were introduced. In all these methods, a reference waveform is compared to a carrier waveform, and the result is used to set 'ON' and 'OFF' times of the switches. In the first method, which is called naturally sampled pulse width modulation, direct comparison results of the two waveforms are used to select when a switch is 'ON' or 'OFF'. However, in order to find transition points from 'ON' to 'OFF' and vice versa, a complex nonlinear equation should be solved. This problem can be solved by using regular sampled pulse width modulation. In this method, the carrier waveform

is sampled and then gets compared to the reference waveform. Then, the concept of space vector pulse width modulation (SVPWM) was described and its relation to regular sampled PWM was discussed.

Chapter 4 - Integration of DC Link Inductor of the Single-Stage Boost Inverter with Photovoltaic Panel

4.1 Introduction

There are several passive components in the configuration of power electronic circuits. Physical structure of these components causes them to have a big size. Therefore, in order to reduce the total size of the circuit, integrating these passive components with other circuit components into a single package seems a legitimate solution. While majority of work in this thesis focuses on boost inverter, the goal of this chapter is to integrate the DC link inductor of the boost inverter with its input voltage source which is assumed to be a photovoltaic panel.

This chapter contains five sections. In Section 4.2, a review of solar panels is presented. In Section 4.3, a boost inverter as an option for connecting renewable energy resources to a local load or the grid is briefly discussed. In Section 4.4, reasons and methods for integrating various electric components with other circuit components are presented and some previous work in this field is discussed. In Subsection 4.4.1, ANSYS Q3D software, which can be used to find the parasitic value of electrical components, is introduced. Astronergy CHSM6610M photovoltaic panel is modeled using this software and is attempted to integrate the DC link inductor of the boost inverter with the photovoltaic panel by modeling the inductor as a copper wire on the back of the panel. Finally, simulation results showing the inductance value gained from three different wiring configurations is presented. In Section 4.5, the chapter conclusion is given.

4.2 Solar Panel

As previously mentioned, one of the sustainable energy resources is solar energy. High-tech solid state technology has enabled humans to design photovoltaic panels which produce DC electricity when sunlight shines on the photovoltaic array. Figure 4-1 shows an Astronergy CHSM6610M photovoltaic panel [19]. As shown in this figure, the panel consists of 60 cells that have been connected in series. While cells in the panel have been connected in series, the current passing through the panel is equal to the current of each cell. Also, panel voltage is equal to voltage of each cell multiplied by the number of cells in the panel. It is of great importance to note that if any cell is shaded, its current will decrease, thus causing decrease of the total panel current (the current of the panel is equal to the minimum current of

cells). In order to solve this shading problem, bypass diodes in parallel with the cells are used. These diodes can bypass shaded cells and prevent the panel current from becoming too small. Figure 4-2 shows the I-V curve corresponding to this panel. Additional information about this panel, such as open circuit voltage, short circuit current, maximum power current, maximum power voltage and maximum power is presented in Table 4-1. When using solar panels, the goal is to operate the panel at its maximum power point. Maximum power point of a photovoltaic panel is defined as the point at which the product of panel voltage and current is at its maximum. The common assumption states that the maximum power point in the I-V curve of a panel is the point where the slope of the line tangent to the curve is -1.

Figure 4-1 Astronergy CHSM6610M Photovoltaic Panel [19]

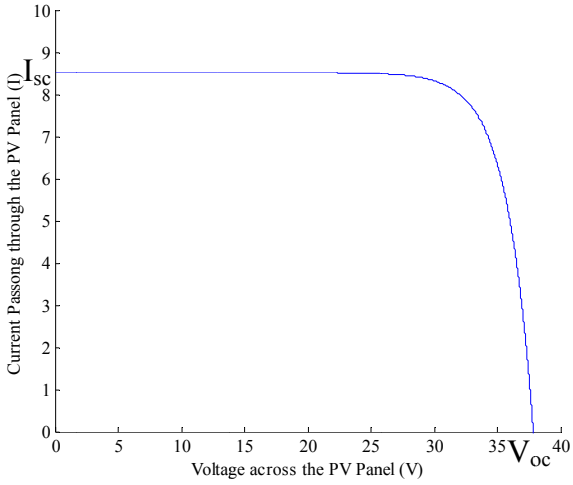


Figure 4-2 I-V Curve of Astronergy CHSM6610M Photovoltaic Panel

Figure 4-2 is at a constant temperature and irradiance level. If these two factors change in any way, the curve will shift up/down or left/right. In other words, if the irradiance level of the sun increases, the short circuit current of the panel will increase and the open circuit voltage will also increase slightly. In addition, if the temperature on the panel surface increases, the open circuit voltage will decrease. Moreover, the short circuit current of the panel will increase

slightly. In order to get maximum possible power from the panel at different environment conditions, panel output is connected to a maximum power point tracker (MPPT) which keeps the operating point of the photovoltaic panel at its maximum power point by using a control strategy. Output of the MPPT can be connected to an inverter converting DC voltage to AC voltage which can be connected to the grid or local load.

Table 4-1 Electrical Specifications of Astronergy CHSM6610M photovoltaic panel [19]

open circuit voltage	37.48 V
short circuit current	8.52 A
maximum power voltage	29.03 V
Maximum power current	7.93 A
Maximum power	230 W

4.3 Power Electronic Interface Circuits between Renewable Energy Resources and Local Load/Grid

Renewable energy resources are connected to the local load or power grid by power electronic interface circuits. Several circuit topologies are available for this application with the most popular being current source inverters (CSI), voltage source inverters (VSI), multilevel inverters, and matrix converters (as discussed in previous chapter).

A single-stage three-phase boost inverter was shown in Figure 2-9. By using a special switching pattern with this inverter, input voltage, which can be the voltage of a photovoltaic panel (DC voltage), can be boosted and output voltage of the inverter is a sinusoidal waveform. The switching pattern, operation, and control strategy used to convert DC input voltage into a sinusoidal waveform will be discussed in future chapters. In order to boost small input DC voltages to desired output voltage (rms line to line of 208v), an inductor with a huge inductance value in the DC side of the circuit is needed. These inductors usually take a lot of space, so integrating this inductor with another component in the circuit would decrease the total size of the circuit.

4.4 Integration of Electric Components in a Circuit

In most of the power converters, passive components such as inductors, capacitors and transformers are the bulkiest parts of the circuit and, therefore, these elements determine the

total size of the circuit. These components usually occupy more than two-thirds of the total space of the circuit, so integration of these passive components is essential and has several advantages such as [20]:

1) It will result in a smaller and more compact circuit.
2) The number of components used in the circuit will be reduced. Therefore, assembly of the circuit will be easier.
3) It will reduce total cost of the circuit.
4) It will increase circuit reliability because wiring no longer exists between the components.
5) Various improvements in electromagnetic interference (EMI) of the system will be made because interconnections between magnetic and capacitive components are reduced.

Based on the reasons mentioned above, integrating passive components with other circuit components into one single package would be useful. For example, in current source boost inverter (shown in Figure 4-3); integrating the photovoltaic panel with the DC-side inductor would be a good solution to reduce circuit size.

Although, no work has previously been done to integrate a photovoltaic panel with a passive component, some research has been done to integrate passive elements into printed circuit board (PCB). In this method, called embedded passives integrated circuit (emPIC), the board consists of several layers that have been laminated on top of each other. Figure 4.4 shows the principle of this method [21].

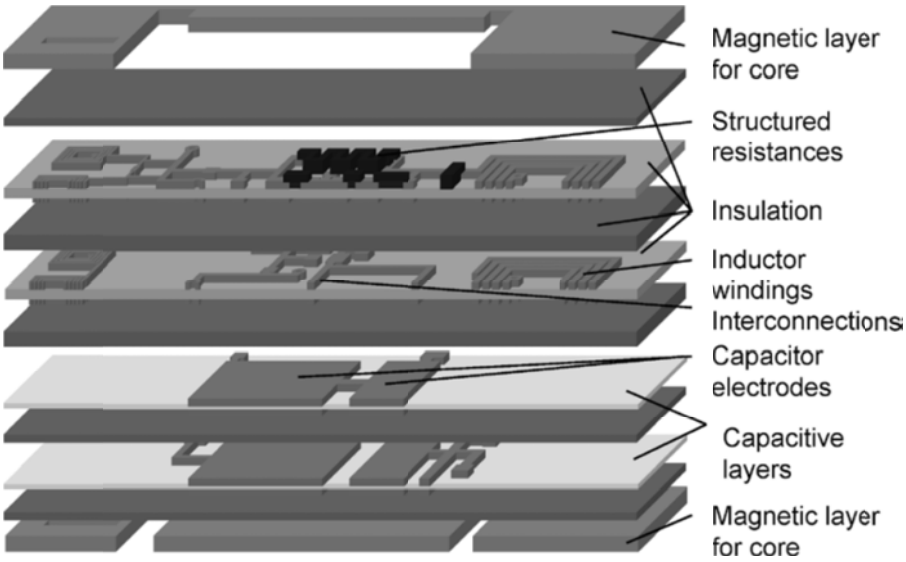


Figure 4-3 Embedded Passives Integrated Circuit Principle [21]

4.4.1 Integration of Capacitors into PCB

Capacitor integration into PCB can be done using capacitive materials as one layer, while two layers of conducting materials on top and bottom of this capacitive layer serve as electrodes for the capacitor. Several technologies can be used for this purpose, making it possible to achieve a capacitance value of $10nF/cm^2$ [22]. Two major technologies for accomplishing this integration are:

1) Using FR4-like laminate with high dielectric powder.

In this method, layers are inexpensive, thick and have low capacity value.

2) Laminating two resin-coated copper foil layers together.

This method will result in thin, expensive layers with high capacity value.

4.4.2 Integration of Magnetic Components into PCB

Magnetic components can be integrated into PCBs by using planar windings. In this case, tracks on PCB are used as windings. Moreover, the magnetic core can be integrated with PCB. This can be done by:

1) Using soft magnetic metal sheets such as NiFe as a separate layer.

While permeability and saturation flux density of these materials are very high, they are very useful in filtering applications. However, because of high conduction level of these materials, high eddy current loss will be present in the core, thus they cannot be used in high frequency applications.

2) Using polymer like materials with ferrite powder (Ferrite Polymer Compound).

These materials are used in high frequency circuits. However, the primary disadvantage of these materials is their huge losses.

4.4.3 Integration of Resistors into PCB

The other electrical component that can be integrated within the PCBs is a resistor. Methods for integrating a resistor with a PCB are [20]:

1) Use of resistive pastes.

This is the most popular method for integrating a resistor with PCB. However, it is not accurate enough and its long term stability is low.

2) Ohmega Ply process.

In this method, a thin layer of high resistive metal is placed between the copper layer and PCB. This method is more precise and stable.

4.5 Q3D Extractor

In order to find the equivalent model of photovoltaic panel and inductor integration, Q3D Extractor software has been used. ANSYS Q3D Extractor software is the premier 3-D and 2-D parasitic extraction tool which can be used to find equivalent resistance, inductance, capacitance, and conductance of electrical components in any circuit. This software uses the method of moments (integral equations) and FEMs to compute these values.

Conventionally, in order to find inductance value, electromagnetic field simulation tools which use finite element analysis (FEA) techniques, are required. However, when the physical structure of the circuit becomes more complex, full field simulation becomes a tedious and extensive task. In this case, partial element equivalent circuit (PEEC) method is used which utilizes Maxwell's integral equations instead of differential equations and calculates an inductance value based on geometry and material information. Q3D extractor is based on PEEC method and has been used in this project to calculate the inductance value [23].

4.5.1 Model Development

An inductor is an electrical component consisting of a conducting material, typically copper wire, wrapped around a core of air or a magnetic material. For this particular research, in order to achieve maximum inductance value and prevent shadowing on photovoltaic cells, the back of the panel has been chosen for wiring. Also, in order to make simulations easier, it has been assumed that the core material for the inductor is air.

The panel used in the simulations is Astronergy CHSM6610M. Information related to cell sizing of this panel has been provided in Table 4-2. Figure 4-5 shows one cell of this photovoltaic panel modeled in Q3D Extractor software.

Table 4-2 Sizing Related to the PV Cell

Symbol	Quantity(mm)
L	155.575
L1	11
W	114.3
W1	38.1
W2	2
H (height of the cell)	0.3
Material	Silicon

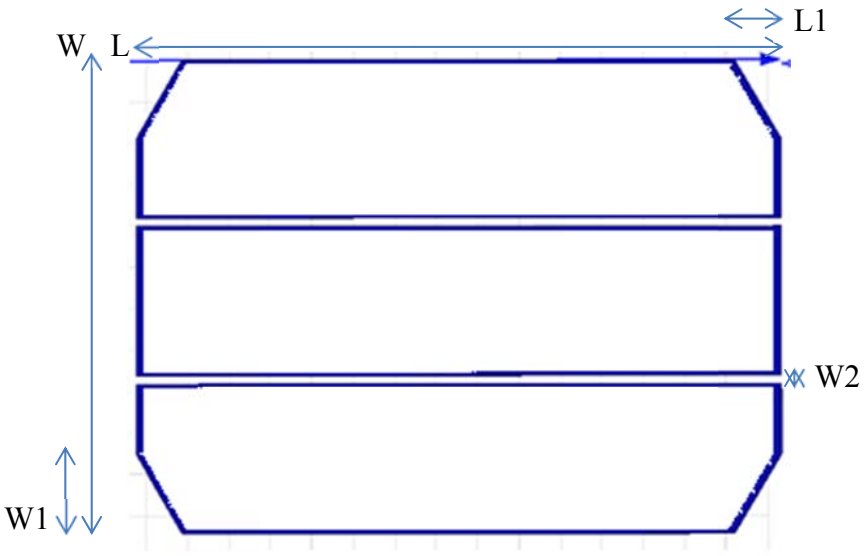


Figure 4-4 Overview of One Cell of Astronergy CHSM6610M Solar Panel

This cell has been used throughout the simulations and three distinct wiring configurations on the back of the cell have been implemented and simulated. For each configuration, the inductance value related to the wiring has been found. It should be noted that the panel consists of 60 cells; therefore, if wiring on the back of all of the cells is done and all of these wirings have been put in series, the total inductance value achieved is approximately sixty times the value achieved in the following simulations.

4.5.2 Simulation Results

In the first wiring configuration, the inductor has been modeled as a copper wire horizontally wound around the back of the photovoltaic panel. This configuration is shown in Figure 4-6 and Sizing related to the copper wire is provided in Table 4-3. Width of the copper wire used to form the inductor equals two times the width of copper wire passing through the photovoltaic panel, and its height equals the height of the copper wire passing through the photovoltaic panel.

Table 4-3 The First Wiring Configuration Information

Symbol	Quantity
Width of copper wire	4 mm
Height of copper wire	0.3-0.6 mm
Distance between wires in consecutive turns	0.05 mm
Distance between PV panel and copper wire	0.1 mm
Number of turns	14
Number of layers	1

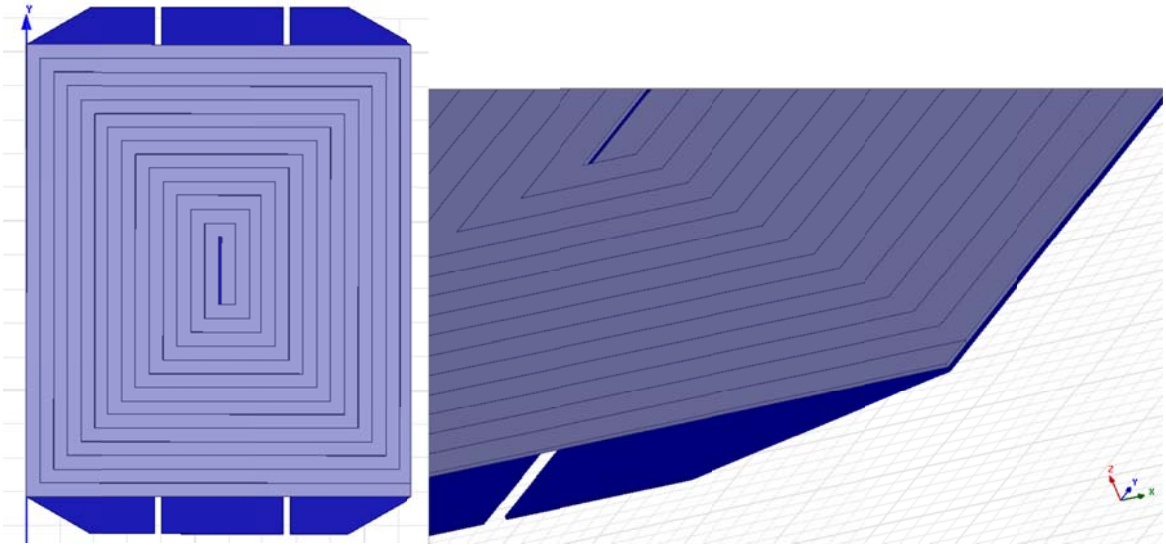


Figure 4-5 First Wiring Configuration

In the simulations, width of the copper wire has been kept constant and its height has been changed from 0.3mm to 0.6mm in step sizes of 0.05 mm. Simulation results for the DC inductance value of the wiring configuration are shown in Figure 4-7. In this figure, the inductance value decreases as the copper wire height increases. Besides, the inductance value reached using this wiring configuration is very small and not usable in power electronic circuits. Therefore, new wiring configurations should be found and simulated to get higher inductance value.

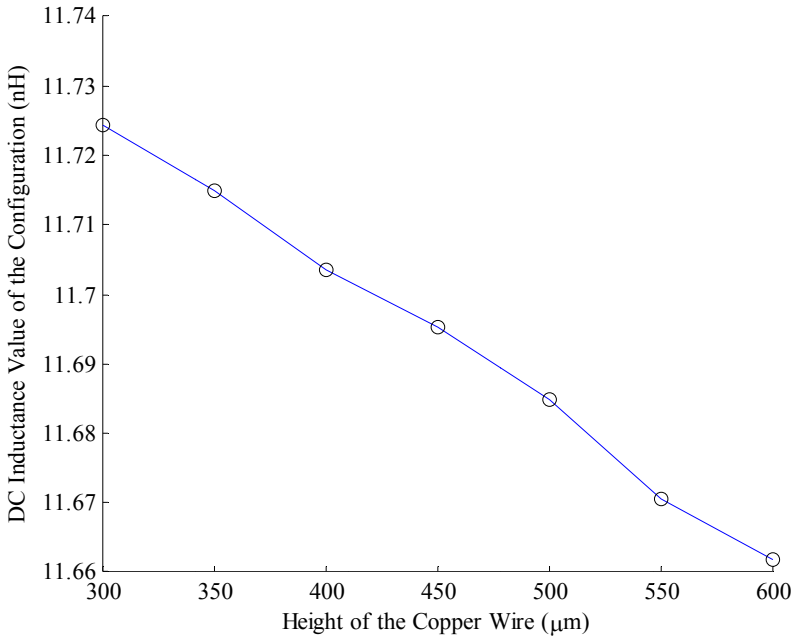


Figure 4-6 First Wiring Configuration Simulation Results

In the second configuration, it has been assumed that the copper wire is going up and down on the back of the photovoltaic panel. This configuration is shown in Figure 4-8 and Additional information about this configuration is provided in Table 4-4.

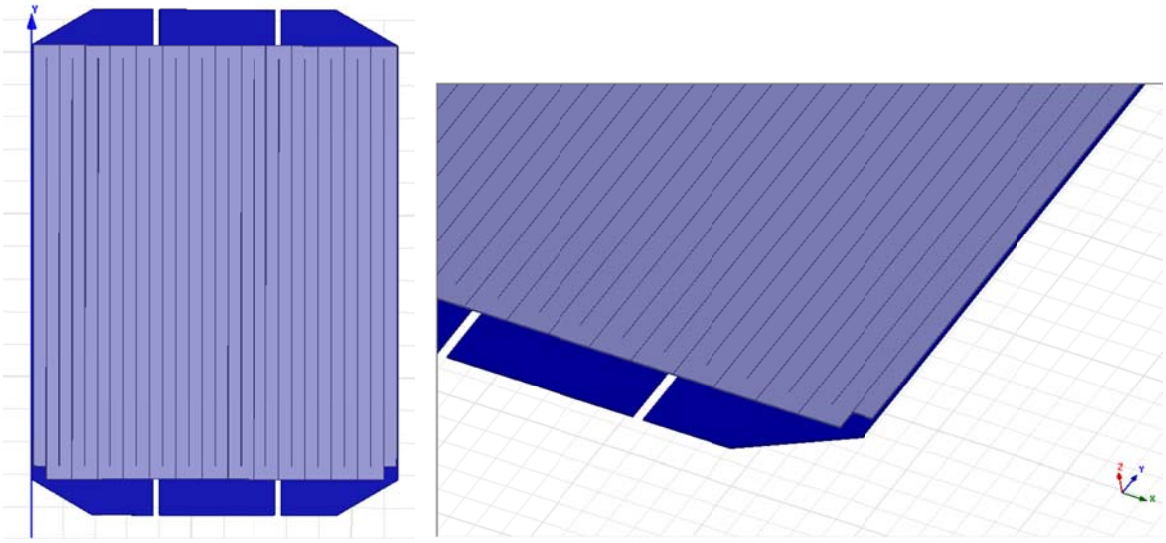


Figure 4-7 Second Wiring Configuration

Table 4-4 The Second Wiring Configuration Information

Symbol	Quantity
Width of copper wire	4 mm
Height of copper wire	0.3-0.6 mm
Distance between wires in consecutive turns	0.05 mm
Distance between PV panel and copper wire	0.1 mm
Number of turns	14
Number of layers	1

In this case, the copper wire height has been changed from 0.3mm to 0.6mm in step sizes of 0.05 mm while width of the copper wire has remained constant. Simulation results for the DC inductance value of the wiring configuration are shown in Figure 4-9. Maximum inductance value can be obtained when the height of the copper wire is at its minimum value. Results show vast improvement over the first case, but the inductance value is not yet an adequate amount.

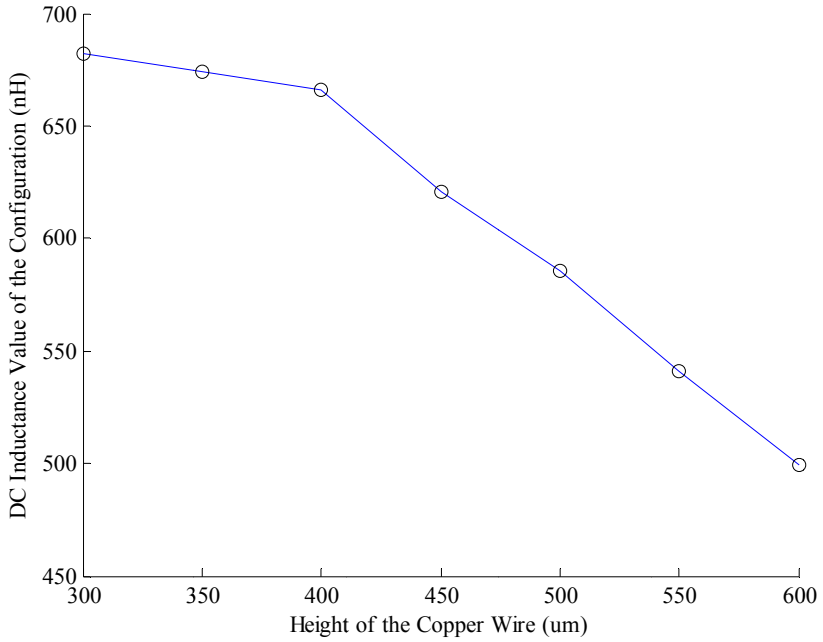


Figure 4-8 Second Wiring Configuration Simulation Results

In the last configuration simulated in this chapter, copper wire has been vertically wound around the back of the photovoltaic panel. This configuration is shown in Figure 4-10 and Table 4-5 summarizes sizing related to wiring in the third configuration.

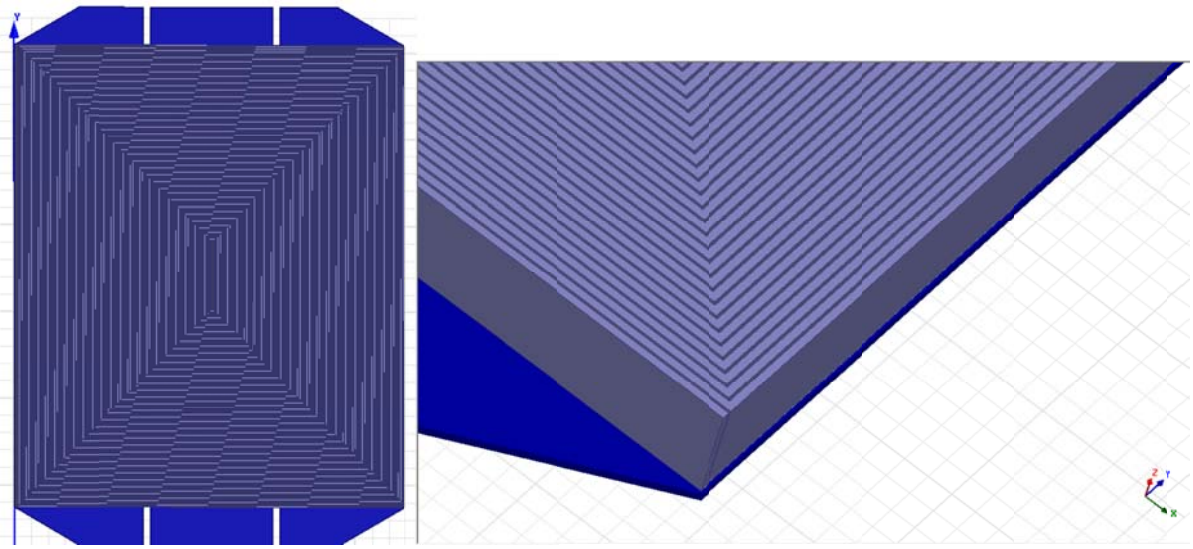


Figure 4-9 Third Wiring Configuration

Table 4-5 The Third Wiring Configuration Information

Symbol	Quantity
Width of copper wire	0.3 mm
Height of copper wire	4-4.2 mm
Distance between wires in consecutive turns	0.1 mm
Distance between PV panel and copper wire	0.1 mm
Number of turns	144
Number of layers	1

In this case, while the number of turns of copper wire was too many, the system could not handle a huge number of simulations; therefore, the wire height was changed from 4mm to 4.2mm with step sizes of 0.1mm. Results of this simulation are shown in Figure 4-11. Results show that the inductance value in this case for each cell is approximately 1.14mH. Therefore, the total inductance value for a panel that has 60 cells (e.g. Astronergy CHSM6610M) will be approximately 68mH, completely fulfilling inverter requirements.

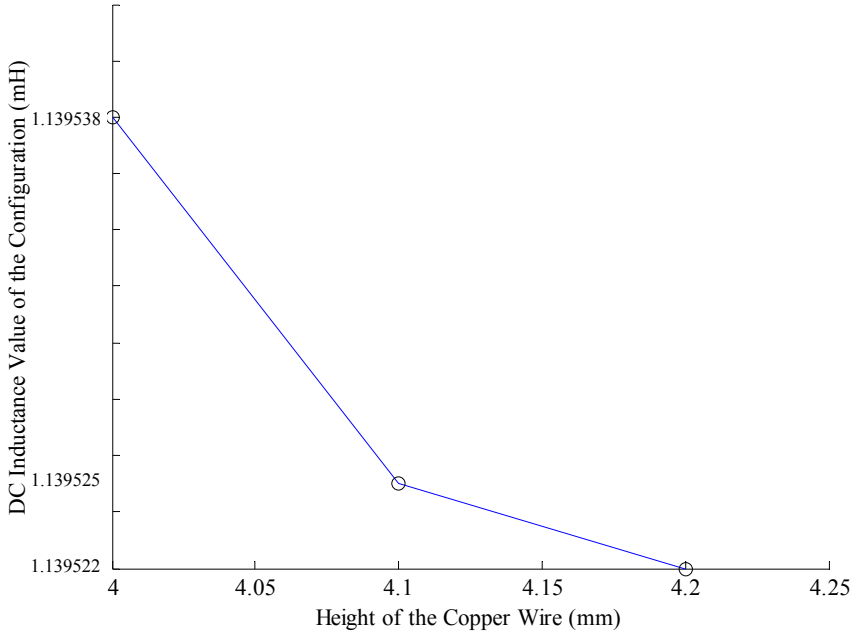


Figure 4-10 Third Wiring Configuration Simulation Results

4.6 Conclusion

In this chapter, integration of a photovoltaic panel with an inductor has been studied. One application of this study is when the goal is to reduce the size of a circuit consisting of a

photovoltaic panel as its input energy source and a boost inverter that has an inductor at its DC side. It has been assumed that Astronergy CHSM6610M photovoltaic panel is connected to a boost inverter with a goal to integrate the panel with the DC-side inductor of the inverter. The panel has been modeled in ANSYS Q3D Extractor based on actual sizing. Also, the inductor has been modeled as a copper wire. Three different configurations of wiring have been designed and simulated to find equivalent DC inductance values of each copper wire. Based on the results, the last configuration provides the highest inductance value which is approximately 1.14mH for each cell.

Chapter 5 - Modified Phasor Pulse Width Modulation

5.1 Introduction

As mentioned in Chapter 2, one interface circuit that can connect a photovoltaic panel to a local load/electric grid is a current source inverter. By using this inverter with a special type of switching pattern and an appropriate control strategy, boosting and inverting input DC voltage into a sinusoidal AC waveform in one stage is possible. The circuit configuration of this inverter, also called a boost inverter is shown in Figure 5-1.

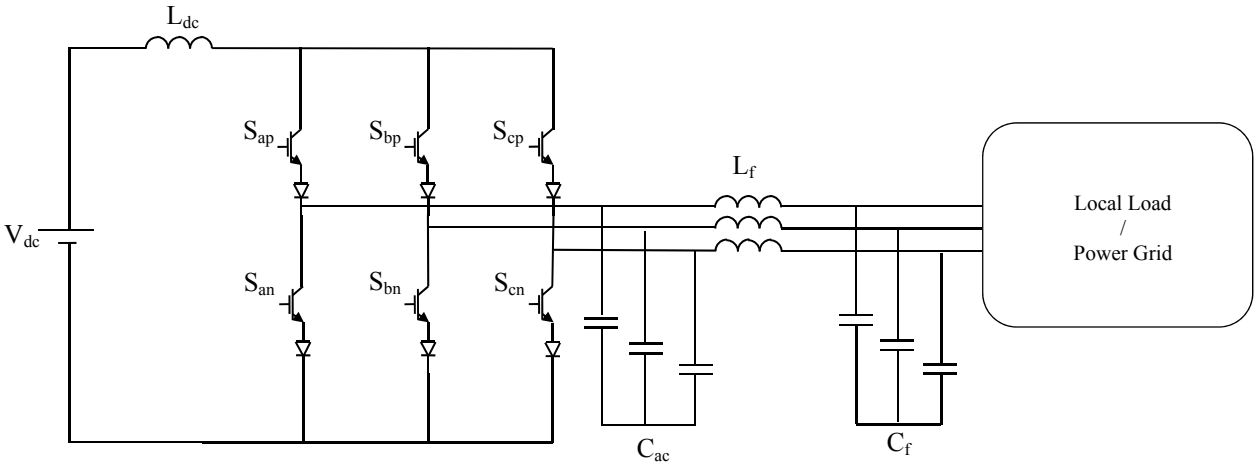


Figure 5-1 Circuit Configuration of a Single-Stage Three-Phase Boost-Inverter

Previously, some studies have been conducted on the application of using current source inverters as a boost inverter for renewable energy systems. In [6], the necessity of a "shoot through" state has been emphasized by using Tri-Level PWM Logic instead of Bi-Level PWM Logic in order to boost input DC voltage to a required peak to peak AC voltage. However, it has been mentioned that because of the switching rate in Tri-Level Logic, loss in this case is more than Bi-Level PWM Logic. In circuit experiments, a large inductor of 100mH and a switching frequency of 1.2 kHz have been used and results show a maximum boost of 3.3 for the ratio of rms line to line voltage to the DC source voltage. In [4], a transformerless three-phase current-source inverter has been presented which provides an output voltage of several hundred volts when its input is connected to a photovoltaic module. Also, it has been mentioned that this inverter can directly be connected to the grid. In this paper, space vector modulation (SVM) has been applied to phase currents of the current source inverter which calculates duty cycles of switching states depending on a reference current vector. These duty

cycles have been calculated based on the assumption that the average value of the DC link current over each switching cycle is constant. The switching frequency used in [4] to do the tests is a relatively high frequency of 25 kHz. Finally, a PI controller has been used in order to control the DC link current. With the descriptions above, the efficiency of the system is approximately 97% and total harmonic distortion (THD) is about 4.5%. In [5], the concept of one cycle control (OCC) has been proposed and then, this concept and also the conventional pulse width modulation method have been used with a current source inverter for grid connection applications. In this paper, the DC inductance value has been kept low (0.55 mH). This would help reduce size, weight, and power dissipation of the inductor which would improve the dynamic response of the system. Also it has been mentioned that using the OCC control method will simplify the control circuit as no microprocessor is necessary in this control algorithm, making the transient response faster and increasing system stability. Moreover, a relatively precise maximum power point tracking (MPPT) function can be integrated with the OCC control system. However, a switching frequency of 40 kHz has been used in [5] which is pretty high for renewable energy conversion systems. By applying the OCC method to an inverter prototype in [5], an efficiency of approximately 92.7% and a total harmonic distortion (THD) of below 5% has been achieved.

This chapter contains three sections. In Section 5.2, phasor pulse width modulation, which is derived based on the concept of space vector pulse width modulation, is defined. Then, this method is applied to a boost inverter which helps determine switches that should be 'ON' at each instant and the duration that each switch should be 'ON'. In Section 5.3, a modified version of phasor pulse width modulation is developed. The reason to use the modified version is that while real systems have a limited step size, they cannot exactly produce the needed time durations. Therefore, some distortions in the output signal will be present due to some asymmetric conditions in the switching pattern of switches (pulse droppings). Modified phasor pulse width modulation is used to prevent these asymmetric conditions. The last section is a conclusion of the chapter.

5.2 Phasor Pulse Width Modulation

In this section, Phasor Pulse Width Modulation (PPWM) which is derived based on the concept of Space Vector Pulse Width Modulation (SVPWM), is defined. It should be noted

that in contrast to SVPWM, the switching pattern in PPWM is developed based on phasor quantities, not space vectors.

In this method, at each instance, one switch from the top row (S_{ap}, S_{bp}, S_{cp}) and one switch from the bottom row (S_{an}, S_{bn}, S_{cn}) is 'ON'. Therefore, there always exists a path for the current of the inductor. Every switching cycle is divided into three parts: one charging state, and two discharging states. During the charging state, both of the switches in the same leg are 'ON', and during each discharging state, one switch from the top row and one switch from the bottom row that are not in the same leg are 'ON', simultaneously. In order to find switches that are 'ON' during each state, the phasor of the output voltage is used.

If the phasor of the output voltage is mapped in a circle, six line to line voltage phasors ($V_{ab}, V_{bc}, V_{ca}, V_{ba}, V_{cb}, V_{ac}$) are used to divide this circle into six sectors, as shown in Figure 5-2. The input DC voltage at each instance falls into one of these sectors. For example, in Figure 5-2, the input voltage (V_{dc}) is in sector I.

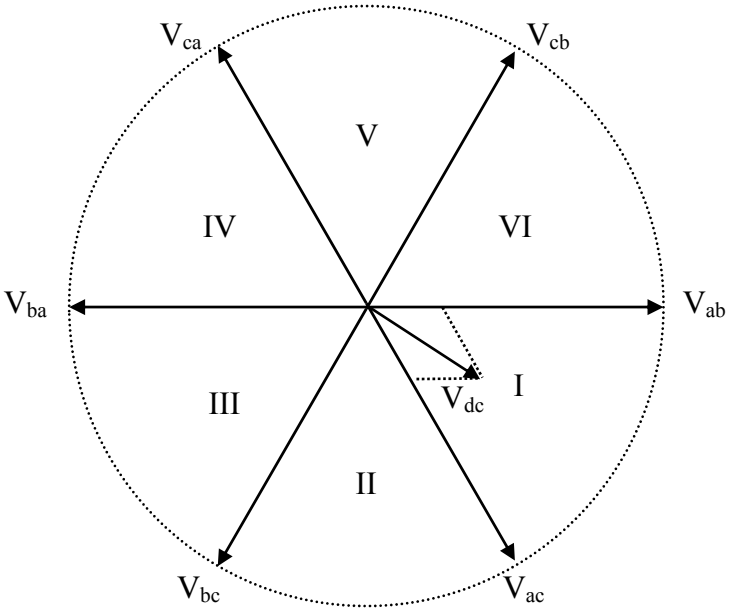
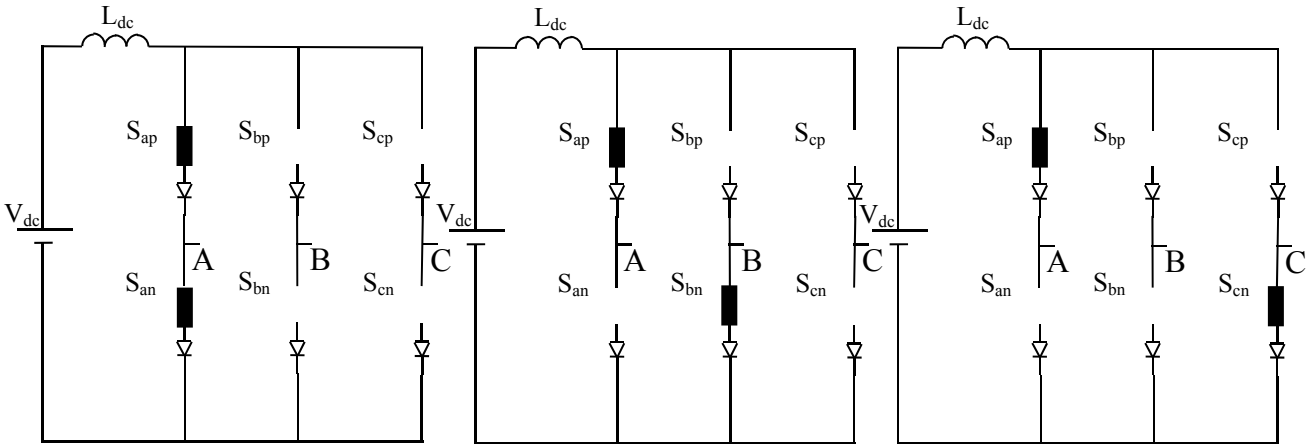


Figure 5-2 Six Sectors Defined Using Line to Line Voltage Phasors

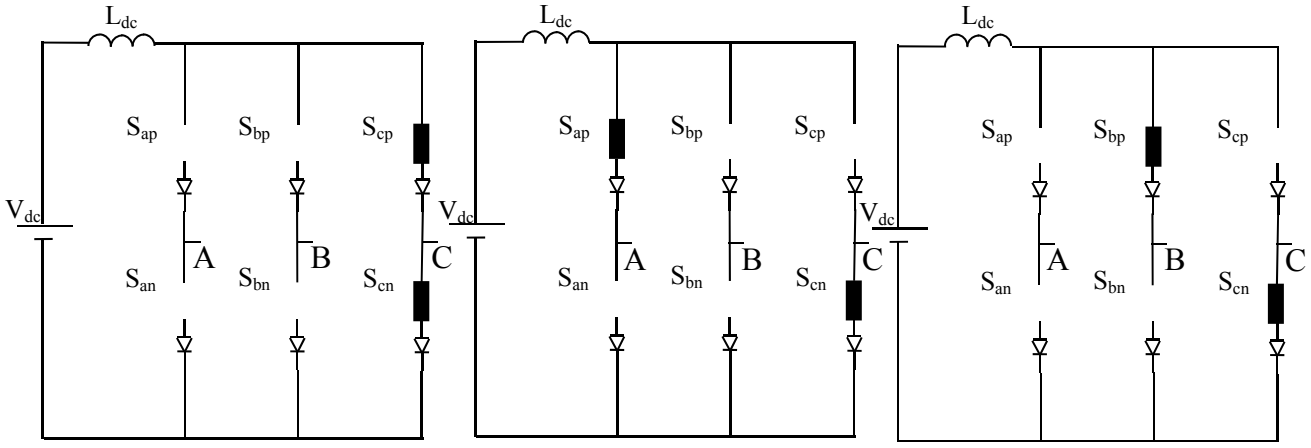
'ON' switches are selected based on the sector containing the DC voltage. The 'ON' switches in each sector are shown in Figure 5-3 and summarized in Table 5-1.

Sector I:



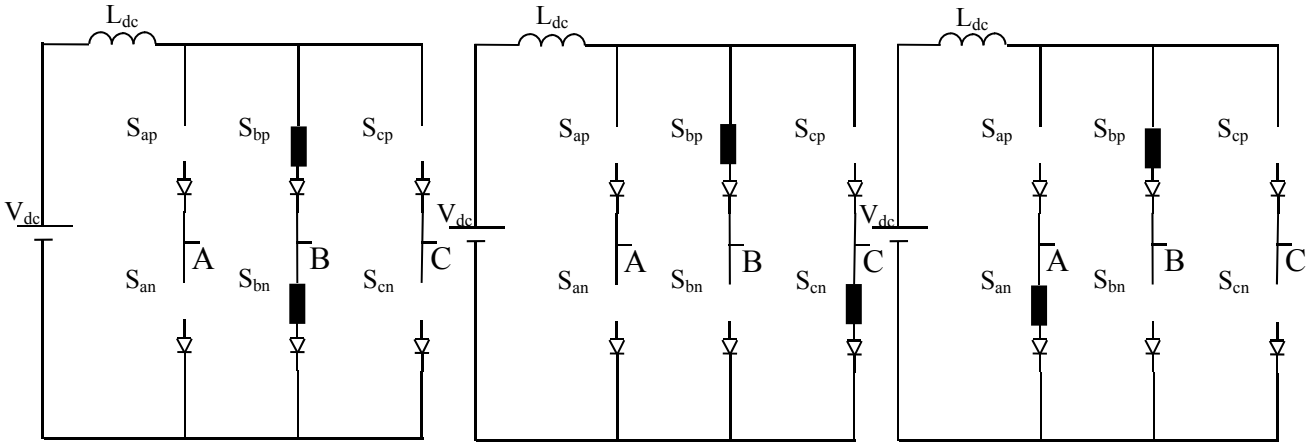
Charging State | Discharging State I | Discharging State II

Sector II:



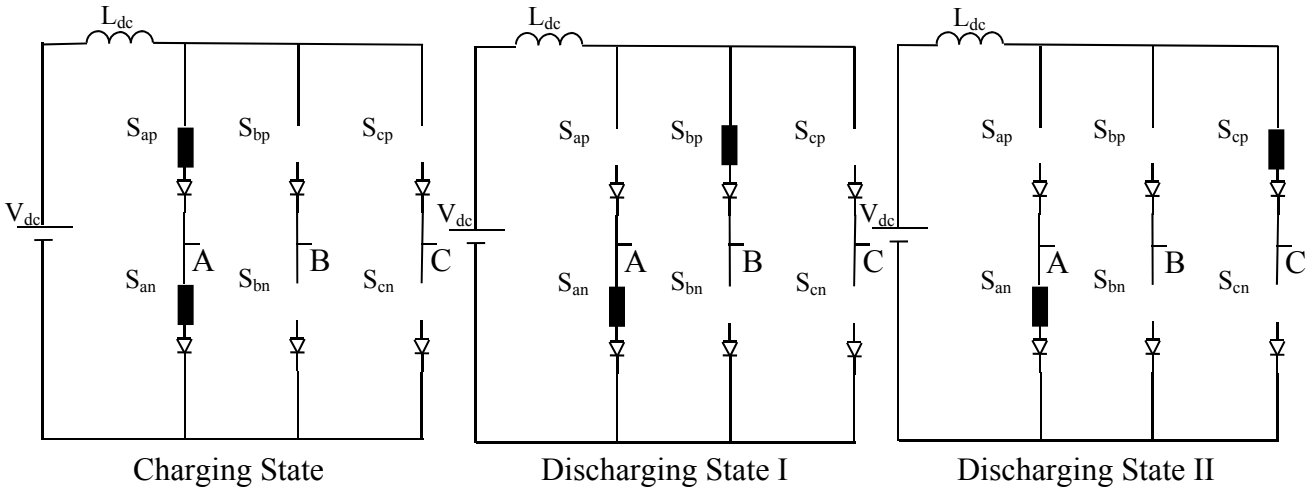
Charging State | Discharging State I | Discharging State II

Sector III:

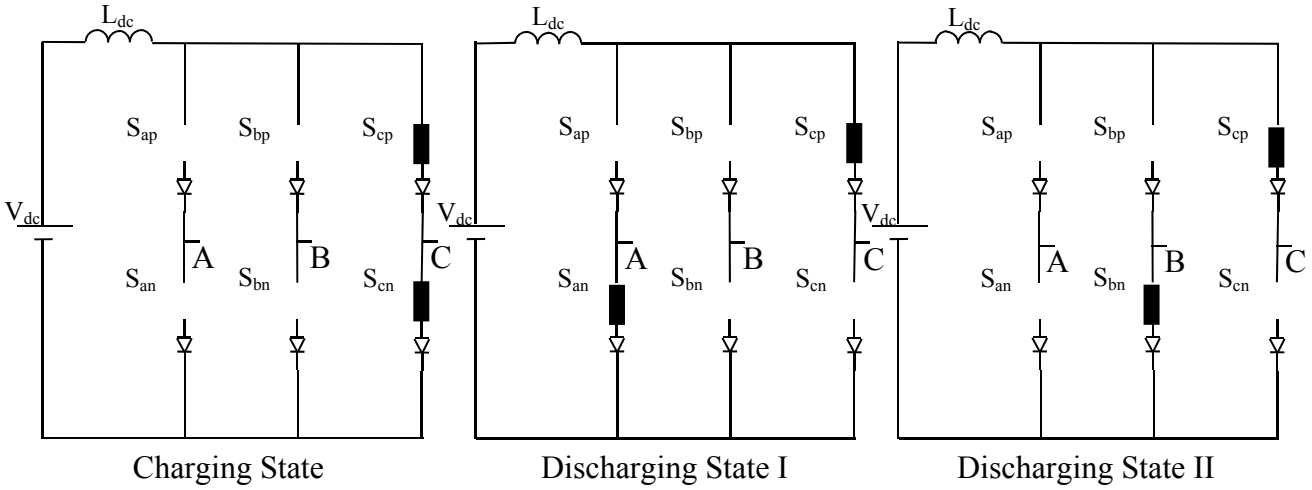


Charging State | Discharging State I | Discharging State II

Sector IV:



Sector V:



Sector VI:

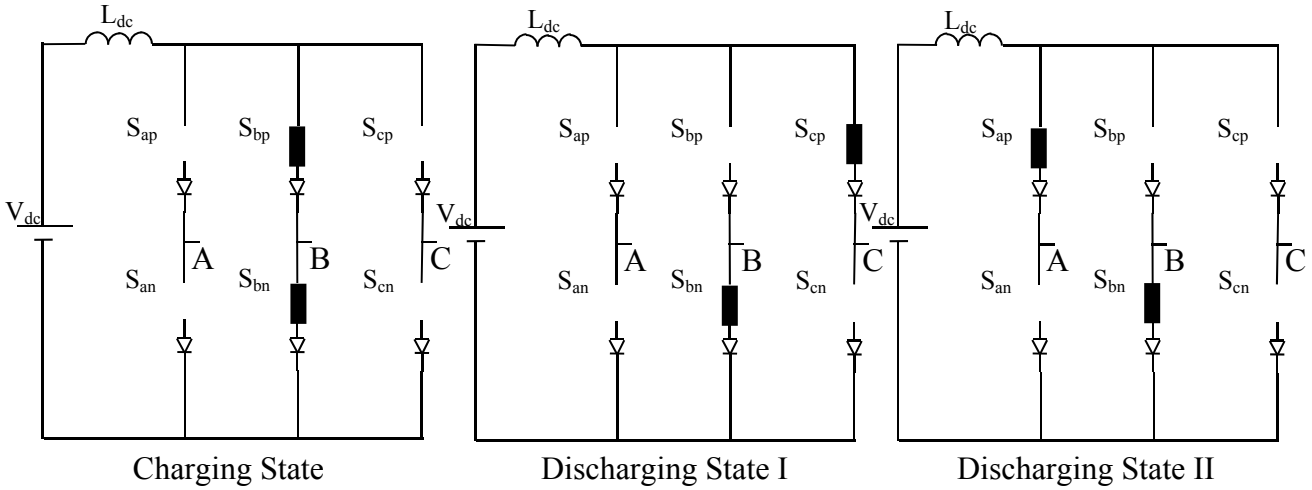


Figure 5-3 Charging and Discharging States of the Boost Inverter in each Section with ON and OFF Switches Shown in each Case

Given the pattern of 'ON' switches at each instant, the next step is to find the total charging and discharging time durations in each switching cycle. Assuming that the input DC voltage stays constant during one switching cycle, the following equations can be written for the DC link inductor voltage and current:

During the charging time,

$$V_L = V_{dc} \tag{5.1}$$

$$I_1 - I_{L_0} = \frac{V_{dc}}{L_{dc}} t_c \tag{5.2}$$

During the first discharging time (assuming the phasor of the output voltage is in sector I),

$$V_L = V_{dc} - V_{ab} \tag{5.3}$$

$$I_2 - I_1 = \frac{V_{dc} - V_{ab}}{L_{dc}} t_{d_1} \tag{5.4}$$

And during the second discharging:

$$V_L = V_{dc} - V_{ac} \tag{5.5}$$

$$I_{LT_s} - I_2 = \frac{V_{dc} - V_{ac}}{L_{dc}} t_{d_2} \tag{5.6}$$

In the above equations, I_{L_0} is the inductor current at the beginning of the switching cycle, I_1 is the inductor current after the charging period, I_2 is the inductor current after the first discharging period and I_{LT_s} is the inductor current after the second discharging period, i.e., at the end of the switching cycle. These equations are summarized in Figure 5-4.

By adding equations (5.2), (5.4), and (5.6), the result is:

$$I_{LT_s} - I_{L_0} = \frac{V_{dc}}{L_{dc}} t_c + \frac{V_{dc} - V_{ab}}{L_{dc}} t_{d_1} + \frac{V_{dc} - V_{ac}}{L_{dc}} t_{d_2} \tag{5.7}$$

This can be written as:

$$I_{LT_s} - I_{L_0} = \frac{V_{dc}}{L_{dc}} \left(t_c + t_{d_1} + t_{d_2}\right) - \left(\frac{V_{ab}}{L_{dc}} t_{d_1} + \frac{V_{ac}}{L_{dc}} t_{d_2}\right) \tag{5.8}$$

By replacing $t_c + t_{d_1} + t_{d_2} = T_s$ and $\Delta I = I_{LT_s} - I_{L_0}$ into equation (5.8), the result is:

$$V_{dc} T_s - \Delta I_L L_{dc} = v_{ab} t_{d1} + v_{ac} t_{d2} \tag{5.9}$$

By assuming that the system is symmetric, the following equations can be written for output voltages:

$$v_{ab}(t) = \sqrt{3} V_m \cos(\omega t) \tag{5.10}$$

$$v_{bc}(t) = \sqrt{3} V_m \cos\left(\omega t - \frac{2\pi}{3}\right) \tag{5.11}$$

$$v_{ca}(t) = \sqrt{3} V_m \cos\left(\omega t - \frac{4\pi}{3}\right) \tag{5.12}$$

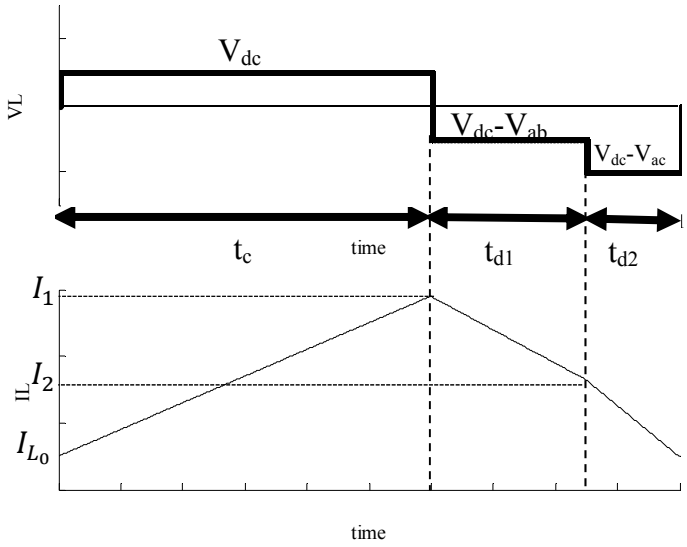


Figure 5-4 Voltage and Current Waveforms of DC Link Inductor in One Switching Cycle

Also, it can be assumed that each discharging period has a duration of:

$$t_{d_1} = k\cos(\alpha) \tag{5.13}$$

$$t_{d_2} = k\cos(\alpha - \tfrac{2\pi}{3}) \tag{5.14}$$

Therefore:

$$v_{ab}t_{d1} + v_{ac}t_{d2} = \sqrt{3}V_m \cos(\omega t)\, k\cos(\alpha) + \sqrt{3}V_m \cos\left(\omega t - \tfrac{4\pi}{3}\right) k\cos\left(\alpha - \tfrac{2\pi}{3}\right) =$$

$$\tfrac{kV_m\sqrt{3}}{2}(\cos(\omega t - \alpha) + \cos(\omega t + \alpha)) + \tfrac{kV_m\sqrt{3}}{2}\left(\cos\left(\omega t - \alpha + \tfrac{\pi}{3}\right) - \cos(\omega t + \alpha)\right) =$$

$$\tfrac{3kV_m}{2}\left(\cos\left(\omega t - \alpha + \tfrac{\pi}{6}\right)\right) \tag{5.15}$$

Substituting equations (5.15) into equation (5.9), the result is:

$$V_{dc}T_s - \Delta I_L L_{dc} = \tfrac{3kV_m}{2}\left(\cos\left(\omega t - \alpha + \tfrac{\pi}{6}\right)\right) \tag{5.16}$$

As demonstrated in equation (5.16), the left side of the equation is independent of time; therefore, the right side should be independent, as well. So, $\omega t - \alpha = \alpha_0$ where α_0 is a constant.

$$V_{dc}T_s - \Delta I_L L_{dc} = \tfrac{3kV_m}{2}\left(\cos\left(\alpha_0 + \tfrac{\pi}{6}\right)\right) \tag{5.17}$$

By finding 'k' from equation (5.17) and substituting it into equations (5.13) and (5.14), discharging times can be found as:

$$t_{d_1} = \frac{2(V_{dc}T_s - \Delta I_L L_{dc})}{3V_m \cos\left(\alpha_0 + \frac{\pi}{6}\right)} \cos(\alpha) = \frac{2(V_{dc}T_s - \Delta I_L L_{dc})}{3V_m \cos\left(\alpha_0 + \frac{\pi}{6}\right)} \cos(\omega t - \alpha_0) \quad (5.18)$$

$$t_{d_2} = \frac{2(V_{dc}T_s - \Delta I_L L_{dc})}{3V_m \cos\left(\alpha_0 + \frac{\pi}{6}\right)} \cos\left(\alpha - \frac{2\pi}{3}\right) = \frac{2(V_{dc}T_s - \Delta I_L L_{dc})}{3V_m \cos\left(\alpha_0 + \frac{\pi}{6}\right)} \cos(\omega t - \alpha_0 - \frac{2\pi}{3}) \quad (5.19)$$

In the steady state condition, the inductor current at the beginning and end of the switching cycle are equal($I_{LT_s} = I_{L_0}$). Also, if it is assumed that $\alpha_0 = -\frac{\pi}{6}$ for ease of calculations, discharging times can be found as:

$$t_{d_1} = \frac{2V_{dc}T_s}{3V_m} \cos(\omega t + \frac{\pi}{6}) \quad (5.20)$$

$$t_{d_2} = \frac{2V_{dc}T_s}{3V_m} \cos(\frac{\pi}{2} - \omega t) \quad (5.21)$$

Given the discharging times, the total charging time can be found by using equation (5.22).

$$t_c = T_s - t_{d_1} - t_{d_2} \quad (5.22)$$

By applying charging and discharging times calculated from equations (5.20), (5.21), (5.22) in every switching cycle to the circuit, a sinusoidal waveform at the output of the circuit can be obtained.

Figure 5-5 shows simulation results for the switching pattern obtained from the above formulas for a system with switching frequency of 2.4 kHz with a step size of 10μs. In this figure, the first row shows the section that the phasor of the output voltage is in and the rest of the figures show the switching pattern that should be applied to S_{ap}, S_{an}, S_{bp}, S_{bn}, S_{cp} and S_{cn}, respectively. The information of Figure 5-5 is summarized in Table 5-1 which shows the 'ON' time of each switch in each section.

Table 5-1 Boost Inverter Switch ON Times in PPWM Method

	ON time of Switches					
Section	S_{ap}	S_{an}	S_{bp}	S_{bn}	S_{cp}	S_{cn}
I	T_{sw}	t_c	0	t_{d1}	0	t_{d2}
II	t_{d1}	0	t_{d2}	0	t_c	T_{sw}
III	0	t_{d2}	T_{sw}	t_c	0	t_{d1}
IV	t_c	T_{sw}	t_{d1}	0	t_{d2}	0
V	0	t_{d1}	0	t_{d2}	T_{sw}	t_c
VI	t_{d2}	0	t_c	T_{sw}	t_{d1}	t_{d2}

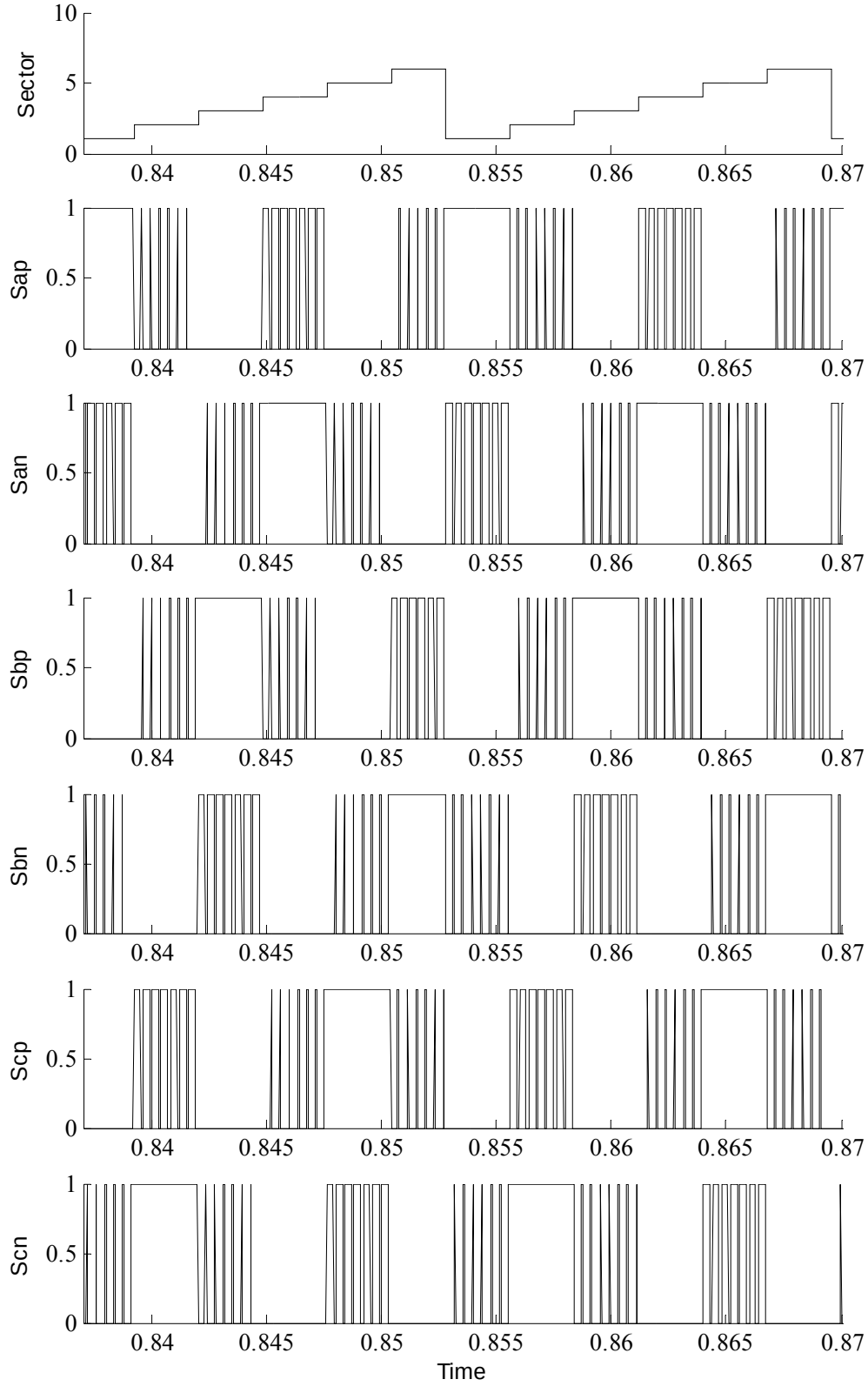


Figure 5-5 Switching Pattern Obtained from Using Phasor Pulse Width Modulation (PPWM)

5.3 Modified Phasor Pulse Width Modulation

As shown in Figure 5-5, every switch is ON for the total length of a special sector and for some periods of time in preceding and subsequent sectors of that sector. However, pulses that show 'ON' times of a switch in those two sectors are not symmetrical. For example, Figure 5-6 shows the magnified switching pattern of S_{ap} in sectors six, one and two. The figure demonstrates that the switching pattern in sectors six and two are not symmetrical. There are 5 pulses in sector six while there are 7 pulses in sector two. These unsymmetrical switching patterns will increase total harmonic distortion (THD) in the output signal.

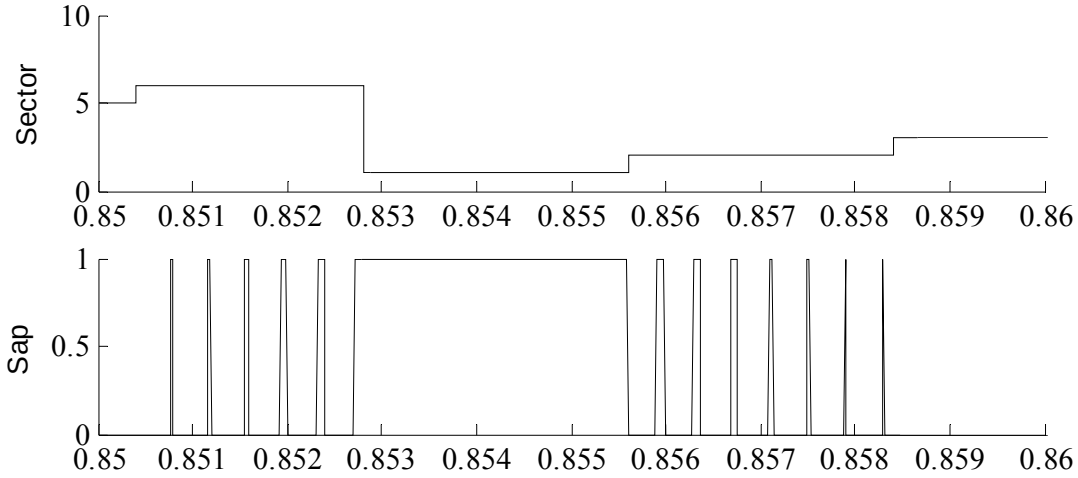


Figure 5-6 Switching Pattern for S_{ap} in Phasor Pulse Width Modulation Method

In order to solve problem, a modified version of phasor pulse width modulation is presented here. Before defining this modified version, however, a brief review of DC-DC boost converter is required.

Circuit topology of a DC-DC boost inverter is shown in Figure 5-7.

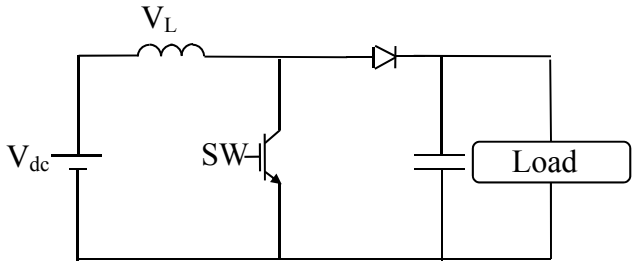


Figure 5-7 DC-DC Boost Converter

Operation of this circuit can be summarized as follows:

1) Switch is on

In this case, the inductor is parallel with the voltage source and therefore:

$$V_{ind} = V_{dc} \tag{5.23}$$

2) Switch is off

In this case, the diode conducts and the inductor is in series with the load, therefore:

$$V_{ind} = V_{dc} - V_{load} \tag{5.24}$$

Voltage across the inductor for one switching cycle is shown in Figure 5-8.

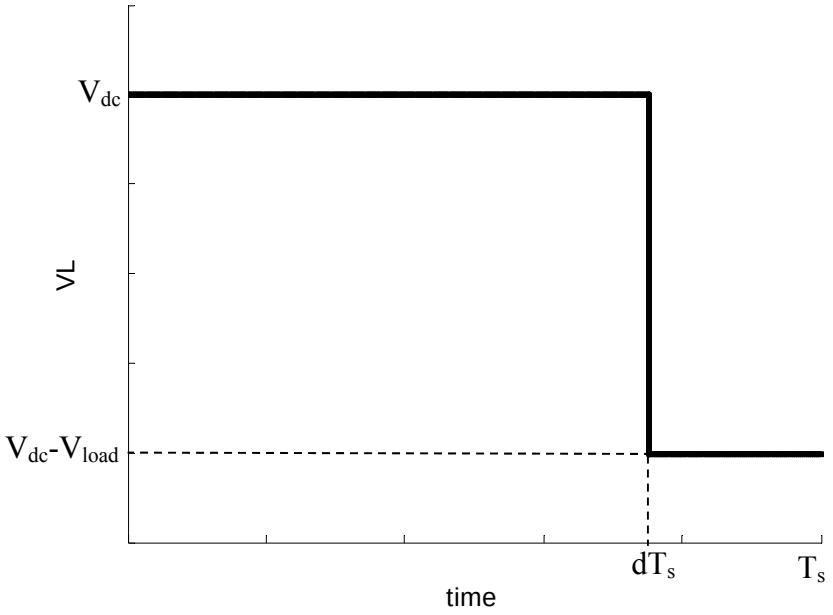


Figure 5-8 Voltage across the Inductor in DC-DC Boost Converter

While integration of inductor voltage over this period should be zero, the following equations can be written. Assuming that the switch is ON for a total length of t_c and the switching frequency is f_s where $T_s = \frac{1}{f_s}$

$$\int V_{ind} = 0 \Rightarrow V_{dc}t_c + (V_{dc} - V_{load})(T_s - t_c) = 0 \Rightarrow \frac{V_{load}}{V_{dc}} = \frac{T_s}{T_s - t_c} \tag{5.25}$$

If the charging ratio is defined as $= \frac{t_c}{T_s}$, the boosting ratio is:

$$\frac{V_{load}}{V_{dc}} = \frac{1}{1-d} \tag{5.26}$$

Comparing the inductor voltages in Figure 5-4 and Figure 5-8, it can be seen that they follow a similar pattern. This idea has been used to develop the modified phasor pulse width modulation.

In the modified phasor pulse width modulation method, results obtained in phasor pulse

width modulation method are discretized; meaning that every switching cycle is described by a preselected number of points; therefore, instead of having time durations for charging and discharging states, these times are presented as a number of points.

In contrast to the phasor pulse width modulation method where discharging times are first found and then, charging time is found by reducing the discharging times from the total switching period, in modified phasor pulse width modulation method, first, the number of points for the charging state is found by multiplying 'd' by the total number of points (N_{total}) and taking the integer part of it as shown in equation 5.27.

$$n_c = floor(d * N_{total}) \tag{5.27}$$

The remaining points should be divided between the two discharging states. Figure 5-9 shows discharging times in the phasor pulse width modulation method in sector I.

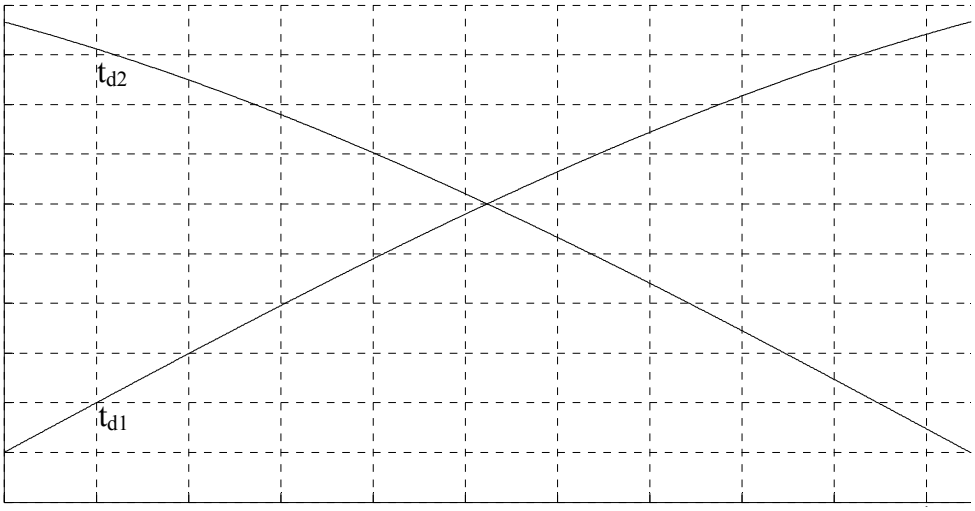


Figure 5-9 Discharging Times in Phasor Pulse Width Modulation Method

As seen in this figure, as one discharging time is increasing (t_{d1}), the other discharging time is decreasing (t_{d2}). Therefore, the number of points associated with these discharging times can be approximated by symmetrical increasing and decreasing steps. If the total number of points in every switching cycle is assumed to be N_{total}, the number of points in every switching cycle associated with the charging time is assumed to be n_c and the number of steps is assumed to be 'n_s' (length of each step is $\frac{\frac{60\pi}{180}}{n_s}$), the amplitude of steps can be found by using equation 5.28 and 5.29.

While the 'floor' function outputs the integer result portion, the possibility exists that, after calculating n_c, n_{d1} and n_{d2}, the sum of these three numbers is not equal to the total number of

points. In order to avoid this, finally, if there is difference between N_{total} and n_c+ n_{d1}+ n_{d2}, this difference is added to n_c as shown in equation 5.30.

$$n_{d1} = floor\left(\frac{k(N_{total}-n_c)}{n_s-1}\right) \qquad k = n_s - 1{:}-1{:}1 \tag{5.28}$$

$$n_{d2} = floor\left(\frac{k(N_{total}-n_c)}{n_s-1}\right) \qquad k = 1{:}1{:}n_s - 1 \tag{5.29}$$

$$n_{c_{final}} = n_c + (N_{total} - n_c - n_{d1} - n_{d2}) \tag{5.30}$$

The steps associated with n_{d1} and n_{d2} have been shown in Figure 5-10 by assuming the total number of steps is 10. This figure shows the symmetric condition in two discharging states, which is the purpose of using modified phasor pulse width modulation.

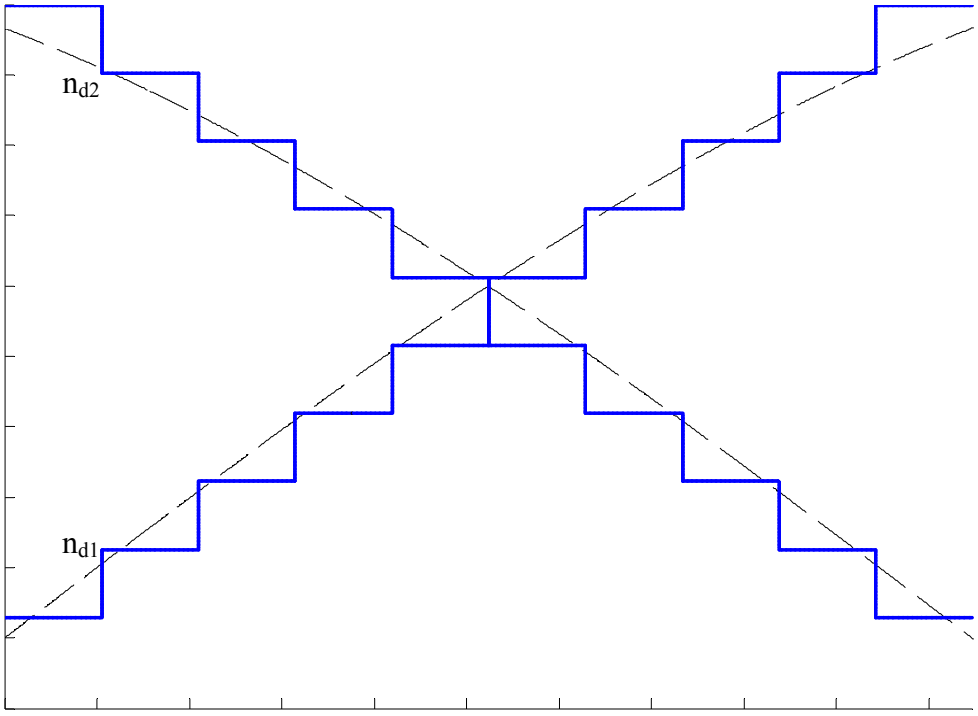


Figure 5-10 Discharging Points in Modified Phasor Pulse Width Modulation Method

Knowing n_c, n_{d1}, n_{d2} and the sector of the system, the switching pattern for each switch can be found. It is exactly the same as using the phasor pulse width modulation method but instead of utilizing time durations for charging and discharging states, the number of points (number of step sizes used in the system) are used to produce charging and discharging states. The switching pattern is shown in Figure 5-11. As seen in this figure, all switching patterns are symmetrical in preceding and subsequent sectors of the sector that a switch is fully 'ON'. This symmetric condition will decrease distortions in the output waveforms.

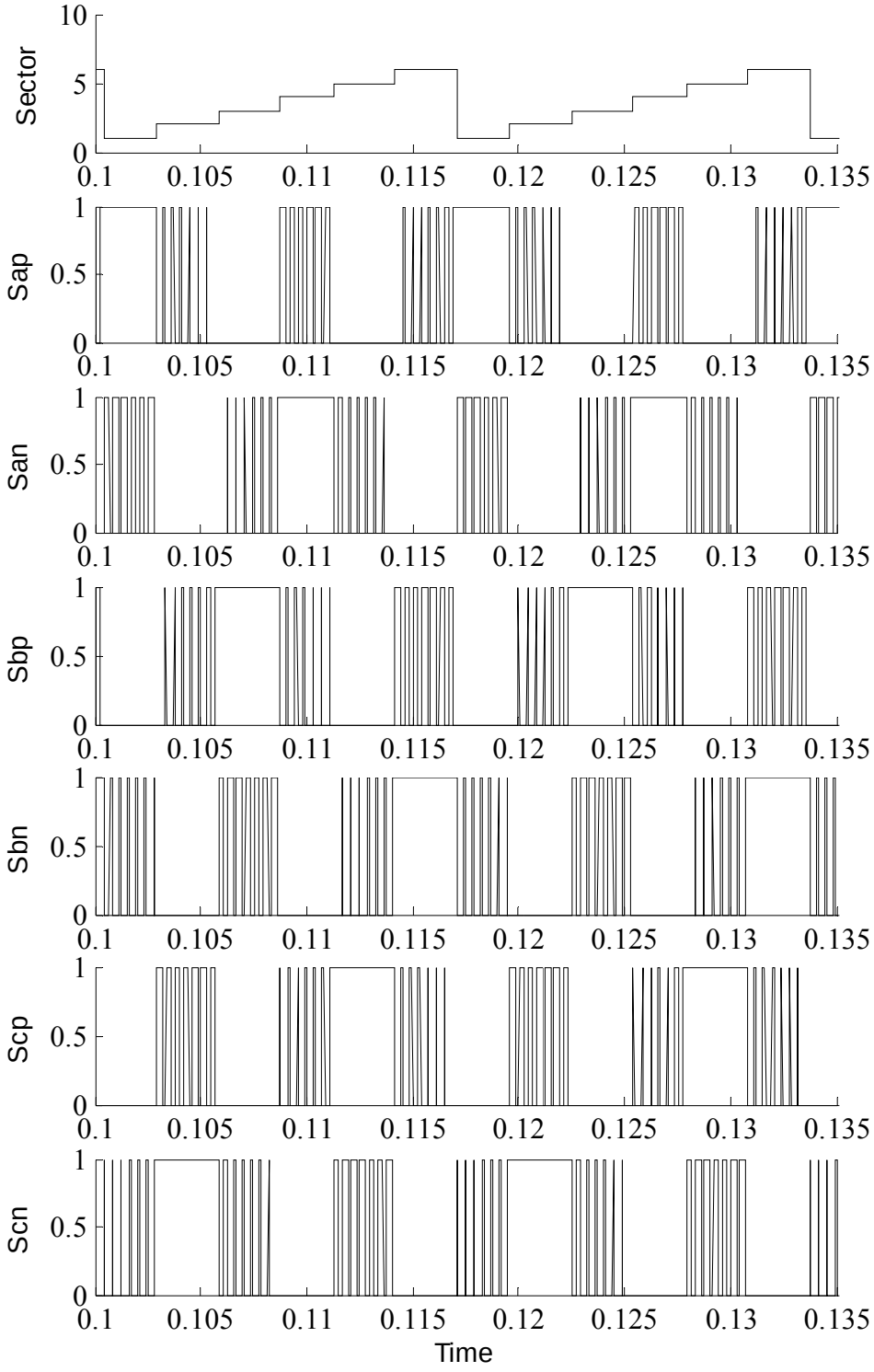


Figure 5-11 Switching Pattern Obtained from Using Modified Phasor Pulse Width Modulation

5.4 Conclusion

In this chapter, phasor pulse width modulation was defined and its use in boost inverter to find switching patterns for six switches was studied. In this method, discharging times are first found based on vector theory and then, charging time is found by reducing discharging times from the switching period. Because unsymmetrical conditions were present in the switching pattern thus increasing the distortions in the output waveforms, a modified phasor pulse width modulation was developed making the switching pattern completely symmetrical. In this method, first, a special number (as the total number of points in each switching period) is assigned to the system. Then, the number of charging points is found by multiplying the total number of points by a charging ratio (defined as 'd'), followed by symmetrical division of the number of points in discharging states. In the next chapter, this switching pattern is used to run the boost inverter in the stand-alone mode.

Chapter 6 - Simulink Model Development and Simulation Results

6.1 Introduction

In this chapter, the Simulink model for applying modified phasor pulse width modulation to a boost inverter in stand-alone mode is developed. This model uses technique introduced in the previous chapter to produce the switching pattern for switches of the inverter. This pattern is used to convert input DC voltage into a sinusoidal waveform at the output. A closed loop control system is used to keep the root mean square of the output line to line voltage at a desired value. At the end of the chapter, simulation results for different values of input voltage and load are presented and a comparison between them is given.

6.2 Simulink Model Development

The Simulink model used to simulate the boost inverter with modified phasor pulse width modulation is shown in Figure 6-1. In this section, different parts of this model will be studied in more detail.

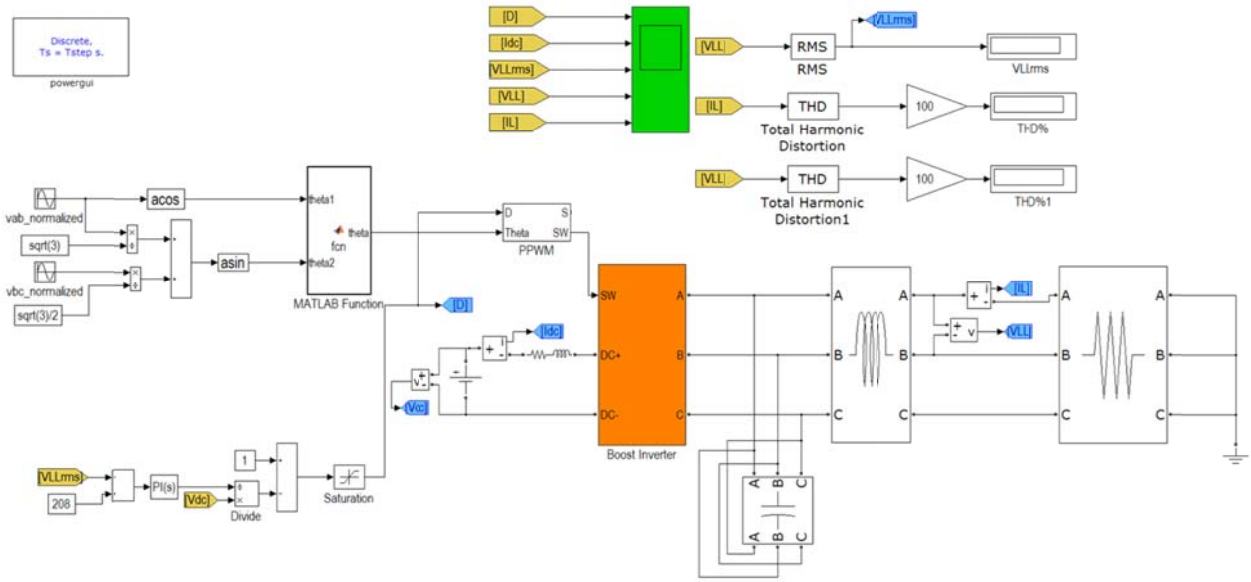


Figure 6-1 Simulink Model of Boost Inverter with Modified Phasor Pulse Width Modulation Switching Method

6.2.1 Phase of Output Signal

The first thing needed in order to be able to use the modified phasor pulse width modulation

method is the phasor of the output signal. Figure 6-2 shows Simulink blocks that have been used to find this phasor. For determining the phasor of the output signal, two output line to line voltages are required. If it is assumed that v_{ab} and v_{bc} are known as:

$$v_{ab}(t) = v_m \cos(\Theta) \tag{6.1}$$

$$v_{bc}(t) = v_m \cos(\Theta - \tfrac{2\pi}{3}) \tag{6.2}$$

Equation (6.1) can be used to find Θ directly.

$$\Theta_1 = \arccos(\frac{v_{ab}(t)}{v_m}) \tag{6.3}$$

However, equation (6.3) gives an angle which is in $[0:\pi]$ interval. In order to have an angle that is changing from 0 to 2π with a frequency of 60Hz, another equation is required.

$$\frac{v_{ab}(t)}{v_m\sqrt{3}} + \frac{v_{bc}(t)}{\frac{v_m\sqrt{3}}{2}} = \frac{\cos(\Theta) + 2\cos(\Theta - \frac{2\pi}{3})}{\sqrt{3}} = \frac{\cos(\Theta) + \cos\left(\Theta - \frac{2\pi}{3}\right) + \cos(\Theta - \frac{2\pi}{3})}{\sqrt{3}}$$

$$= \frac{\cos\left(\Theta - \frac{\pi}{3}\right) + \cos(\Theta - \frac{2\pi}{3})}{\sqrt{3}} = \cos\left(\Theta - \frac{\pi}{2}\right) = sin(\Theta) \tag{6.4}$$

Therefore,

$$\Theta_2 = \arcsin(\frac{v_{ab}(t)}{v_m\sqrt{3}} + \frac{2v_{bc}(t)}{v_m\sqrt{3}}) \tag{6.5}$$

Equation (6.5) gives an angle which is in $[-\frac{\pi}{2}:\frac{\pi}{2}]$ interval.

Results of both equations (6.3) and (6.5) can be used to find the correct angle.

1) If $\Theta_1 \leq \frac{\pi}{2}$ and $\Theta_2 \geq 0$

   $\Theta = \Theta_1$ (6.6)

2) If $\Theta_1 \leq \frac{\pi}{2}$ and $\Theta_2 \leq 0$

   $\Theta = 2\pi + \Theta_2$ (6.7)

3) If $\Theta_1 \geq \frac{\pi}{2}$ and $\Theta_2 \geq 0$

   $\Theta = \Theta_1$ (6.8)

4) If $\Theta_1 \geq \frac{\pi}{2}$ and $\Theta_2 \leq 0$

   $\Theta = \pi - \Theta_2$ (6.9)

By using equations (6.6) through (6.9), the angle of the output signal can be found, as shown in Figure 6-3. This figure demonstrates that the phasor of the output signal is changing

in [0:2π] interval with a frequency of 60Hz.

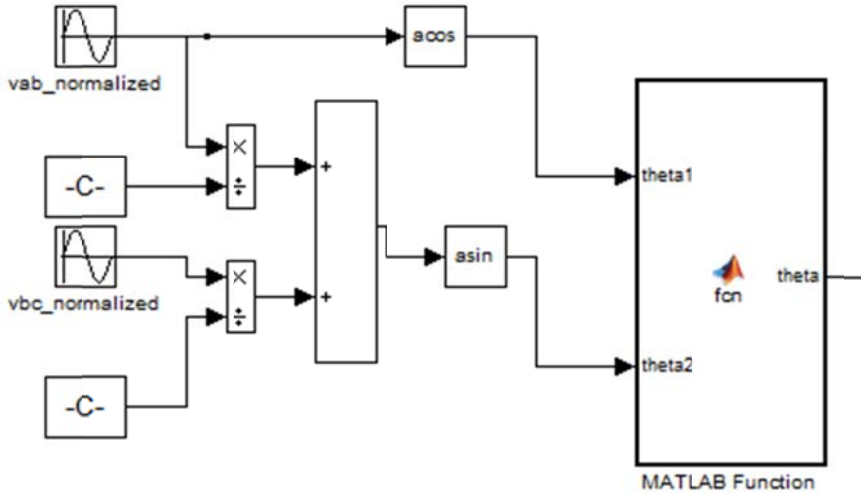


Figure 6-2 Simulink Blocks Used to Find the Phase of the Output signal

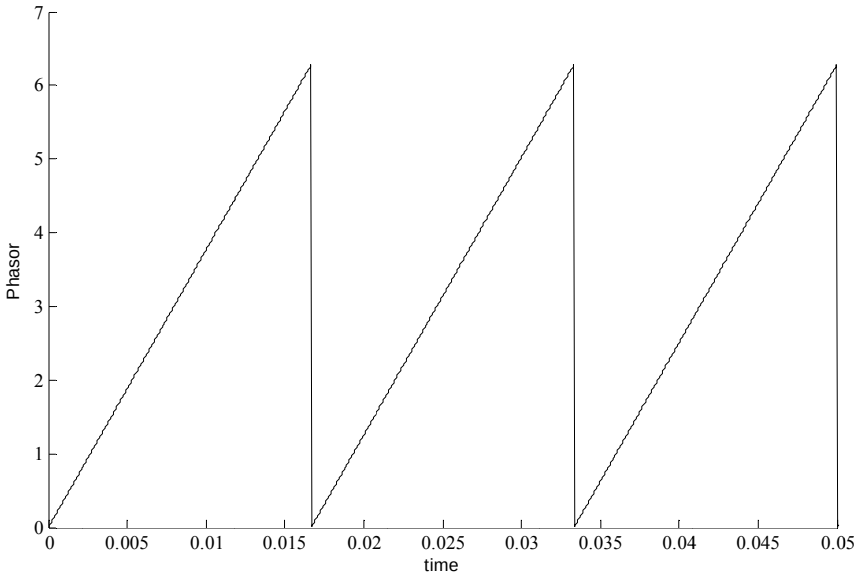


Figure 6-3 Phase of the Output Signal

6.2.2 Switching Pattern

By having the phasor of the output waveform, the next step is to determine switching pattern for switches in the boost inverter. Figure 6-4 shows Simulink blocks used to determine the switching pattern. All these blocks have been masked under the 'PPWM' block in the main Simulink model.

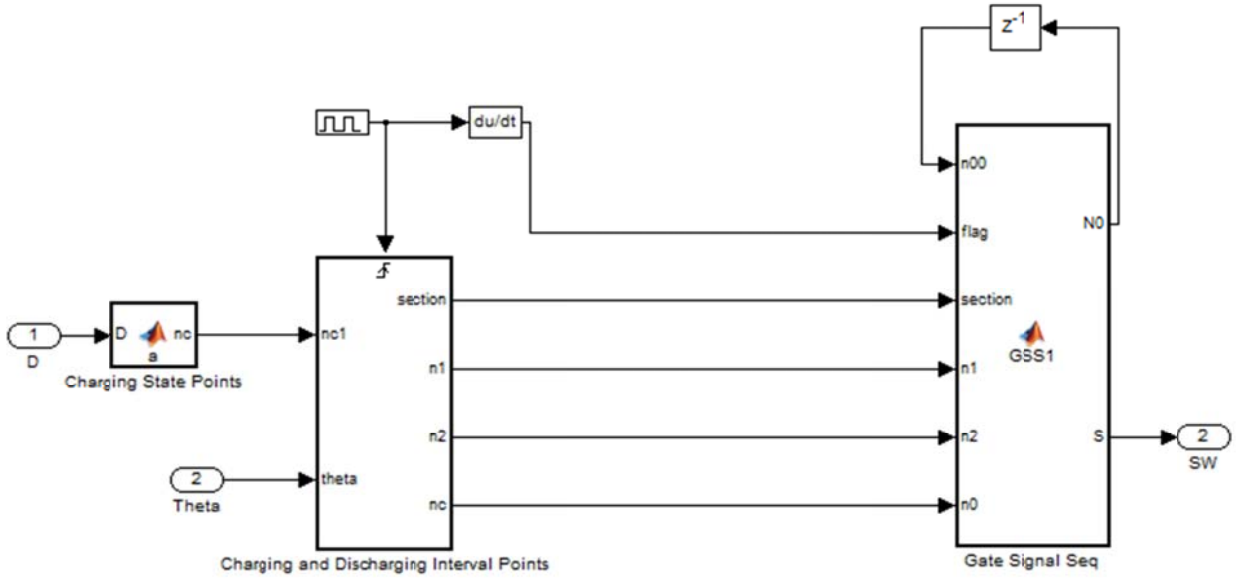


Figure 6-4 Simulink Blocks Used to Find the Switching Pattern

Inputs of the 'PPWM' block are 'D' and 'Theta'. 'D' is output of the control system (which will be discussed further in subsection 6.2.3), and 'Theta' is the phasor of the output signal (previously discussed in subsection 6.2.1). First, the number of points associated with the charging state is determined by 'Charging State Points' block. The number of points is determined by using equation (5.10) below.

$$n_c = floor(N_{total} * D) \tag{6.10}$$

'Theta', along with n_c found above, are inputs of 'Charging and Discharging Interval Points' block. This block is activated by the rising edge of a square waveform with a frequency of f_{pwm} (switching frequency), meaning that this block runs once every $T_{pwm} = \frac{1}{f_{pwm}}$ seconds and outputs are 'section', 'n_1', 'n_2' and 'n_c'.

In this block, the sector of the phasor of the output signal is determined.

1) $0 \leq \Theta \leq \frac{\pi}{3}$ sector→1 (6.11)

2) $\frac{\pi}{3} \leq \Theta \leq \frac{2\pi}{3}$ sector→2 (6.12)

3) $\frac{2\pi}{3} \leq \Theta \leq \frac{3\pi}{3}$ sector→3 (6.13)

4) $\frac{3\pi}{3} \leq \Theta \leq \frac{4\pi}{3}$ sector→4 (6.14)

5) $\frac{4\pi}{3} \leq \Theta \leq \frac{5\pi}{3}$ sector→5 (6.15)

6) $\frac{5\pi}{3} \leq \Theta \leq \frac{6\pi}{3}$ sector→6 (6.16)

After finding the sector (section) that the system is in, the number of charging and discharging points should be found by using the discussion on modified phasor pulse width modulation in the previous chapter. In the Simulink model, it has been assumed that the number of steps for discharging steps is 10. Therefore, the number of points associated with discharging states is found by using equations (6.17) and (6.18). While there is a possibility that by using the floor function, the total number of points (N_{total}) is not equal to the sum of charging and discharging points ($n_c+n_{d1}+n_{d2}$), the difference of these two numbers is added to n_c as shown in equation (6.19).

$$n_{d1} = floor\left(\frac{k(N_{total}-n_c)}{9}\right) \qquad k = 9:-1:1 \tag{6.17}$$

$$n_{d2} = floor\left(\frac{k(N_{total}-n_c)}{9}\right) \qquad k = 1:1:9 \tag{6.18}$$

$$n_{c_{final}} = n_c + (N_{total} - n_c - n_{d1} - n_{d2}) \tag{6.19}$$

These four signals, along with 'flag' and 'n00', are the input signals of 'Gate Signal Seq' block, and its outputs are six signals, which are gate signals, that should be applied to switches.

This block uses a counter which changes from 0 to N_{total} in every switching cycle and goes to zero at the beginning of the next cycle. The 'flag' input controls this input. Whenever rising edge of the square waveform occurs, the flag becomes nonzero and the counter goes to zero, otherwise, flag is zero and the counter increments by one at every step. The assumption has been made that in every switching cycle, first the charging state and the two discharging states occur. Therefore, at every step, the counter is compared to 'n_c'. If it is less than 'n_c', the system is in charging state, therefore, based on the sector that the system is in, the proper switches are turned on. If the counter is more than 'n_c', the system is in one of the discharging states and therefore, the counter is compared to 'n_c+n_{d1}'. If this condition is true, the system is in its first discharging state and therefore, the proper switches are turned on based on the system sector. If this condition is not true, the system is in its second discharging state and therefore, the proper switches are turned on. Switches that should be turned on in each case can be found in Figure 4-3. The output of the 'Gate Signal Seq' is applied to switches in the boost inverter.

6.2.3 Control System

The final goal of the system is to keep the root mean square value of the line to line voltage at a desired value. In order to do this, a control system is required which compares the

rms value of the output line to line voltage at each instance to the desired value (208 volts), and gives an output signal which is the charging ratio associated with the switching pattern. For example, if the rms value of the output voltage is more than 208 volts, the control system decreases 'd' and vice versa. Figure 6-5 shows Simulink blocks used to control the rms value of the output line to line voltage.

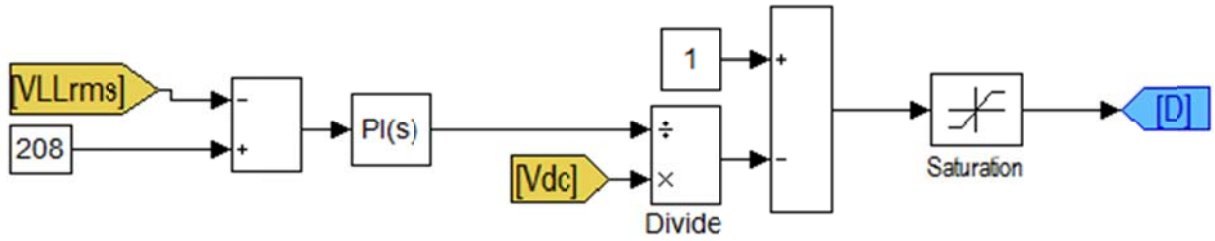


Figure 6-5 Simulink Blocks Used to Control the RMS Value of Line to Line Output Voltage

As derived in equation (5.26), in a DC-DC boost converter, the ratio of output to input voltage was equal to $\frac{1}{1-d}$. By assuming that the boost inverter operates in a similar way to the boost converter, it can be said that the ratio of rms line to line voltage to input DC voltage is equal to $\frac{1}{1-d}$. Therefore,

$$\frac{v_{ll_{rms}}}{v_{dc}} = \frac{1}{1-d} \Rightarrow d = 1 - \frac{v_{dc}}{v_{ll_{rms}}} \tag{6.20}$$

In Figure 6-5, the real rms value is compared to 208 volts, which is the desired rms line to line voltage. A PI controller is used to control the system. The integration part in PI controller makes the error zero. At the end, a saturation block has been used to keep the charging ratio in the range of [0.05:0.95]. This block is necessary to prevent any overvoltage in the system. As the charging ratio increases and gets closer to one, based on equation (6.20), the rms line to line voltage gets bigger and if 'D' becomes equal to one, this rms value goes to infinity (which could cause overvoltage in real systems and burn the switches). Therefore, it is limited to prevent this problem.

6.2.4 Inverter Circuit

Figure 6-6 shows the boost inverter model in Simulink file. This model is identical to the circuit in Figure 5-1.

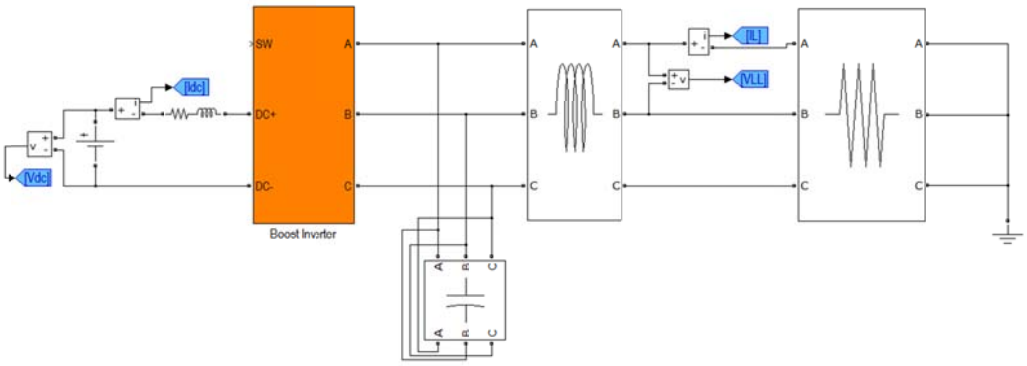


Figure 6-6 Simulink Blocks Used to Model the Boost Inverter

The input is a DC voltage source which has been connected to the inverter in series with an inductor. The output three phase of the inverter have been connected to three capacitors (which have been connected in Δ configuration) and also to three line inductors which act as filter. The output of the filter has been connected to a three-phase load.

In the next section, this Simulink model will be simulated for different input voltages and loads, and results will be presented.

6.3 Simulink Model Results

In this section, results of Simulink model developed in the previous section are presented. Parameter values in the circuit are given in Table 6-1. In the following subsections, results for different circuit component values are given. At the end, a comparison between different cases is presented.

Table 6-1 Simulink Model & Circuit Component Values

Parameter	Value
V_{dc}	50-80 volts
L_{dc}	10mH
C_{ac}	10μF & 20μF
L_{filter}	7.5mH
Load	Resistive Load: 75-100Ω Resistive-Inductive Load: R_L=50Ω & L_L=20mH
f_{sw}	2.4kHz
N_{total}	41
step size	$\frac{1}{f_{sw} * N_{total}}$

6.3.1 Simulation Results for V_{dc}=50V

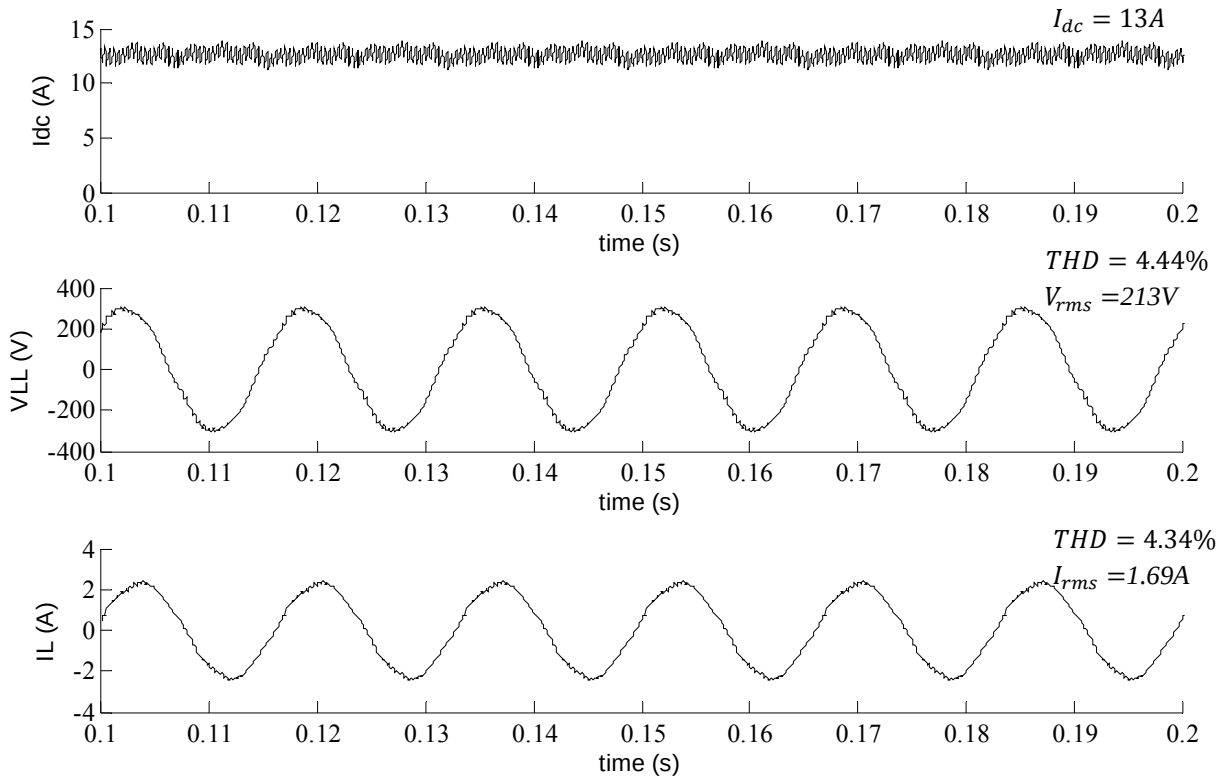


Figure 6-7 Simulation Results for V_{dc}=50V, C_{ac}=10µF and R_{load}=75Ω

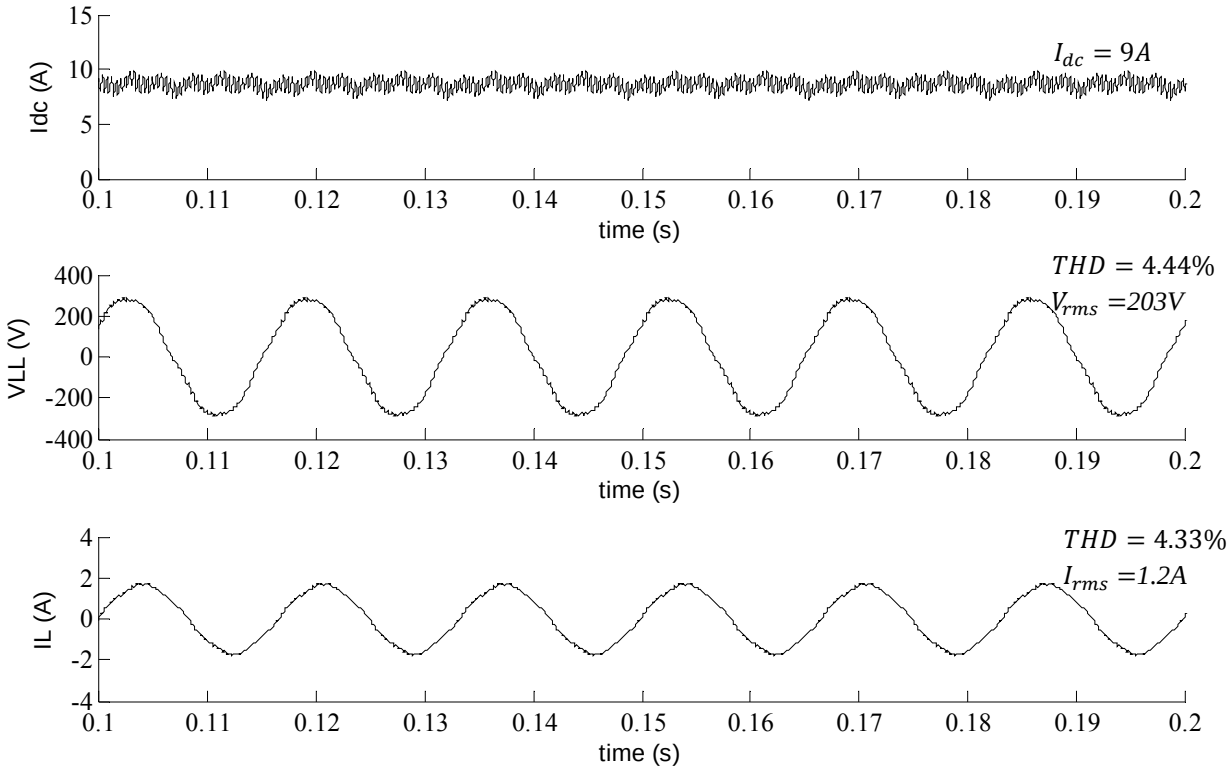


Figure 6-8 Simulation Results for V_{dc}=50V, C_{ac}=10µF and R_{load}=100Ω

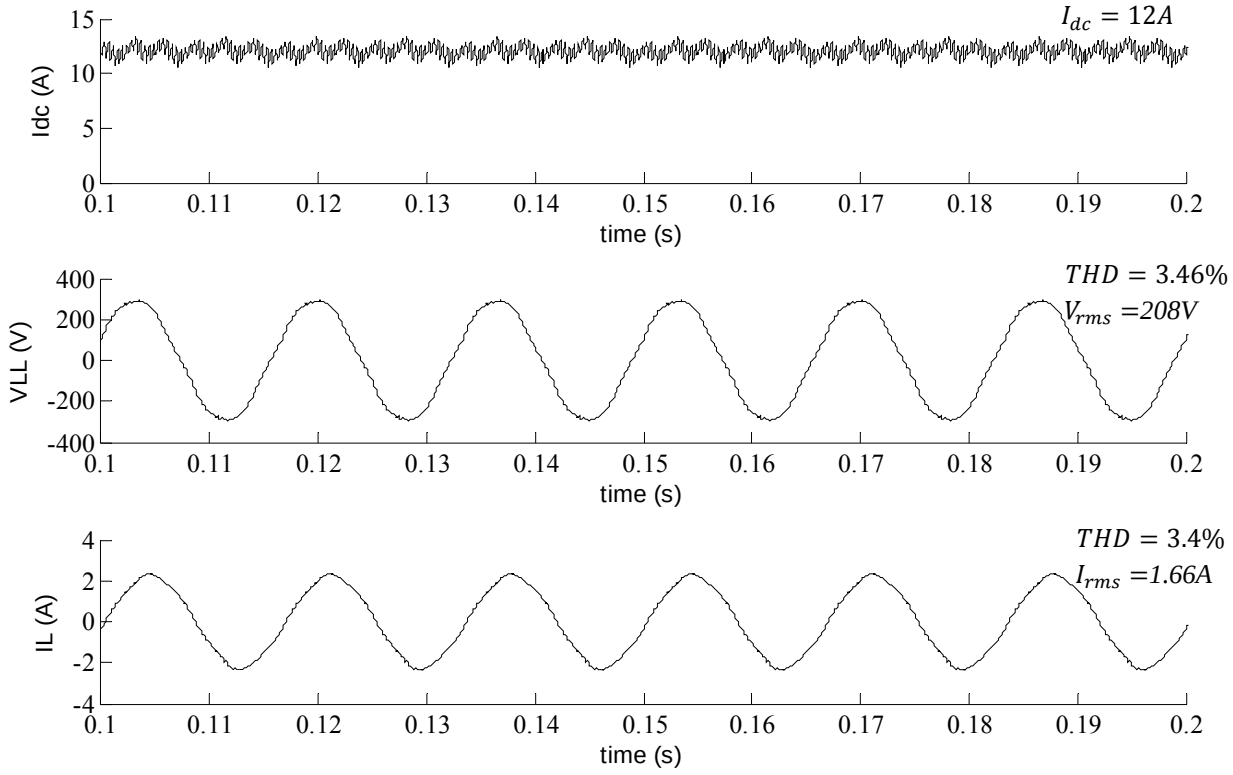


Figure 6-9 Simulation Results for V_{dc}=50V, C_{ac}=20µF and R_{load}=75Ω

6.3.2 Simulation Results for V_{dc}=55V

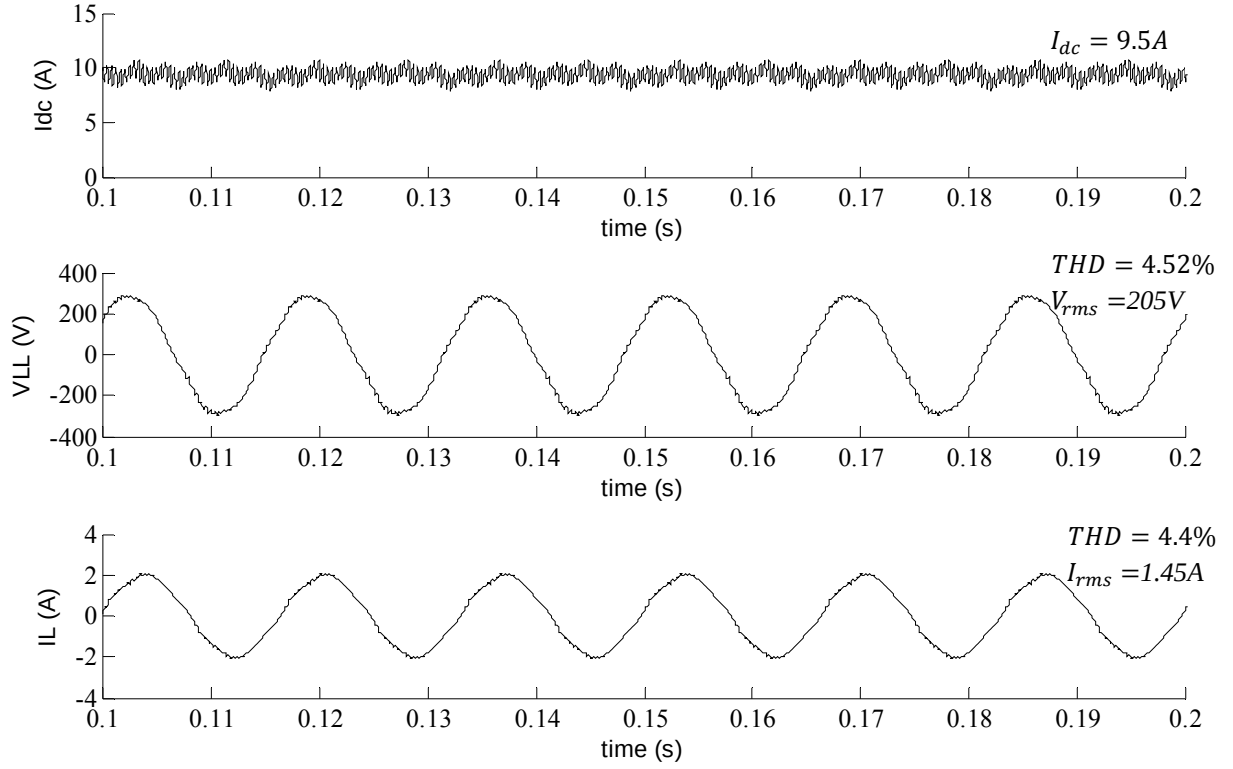


Figure 6-10 Simulation Results for V_{dc}=55V, C_{ac}=10µF and R_{load}=85Ω

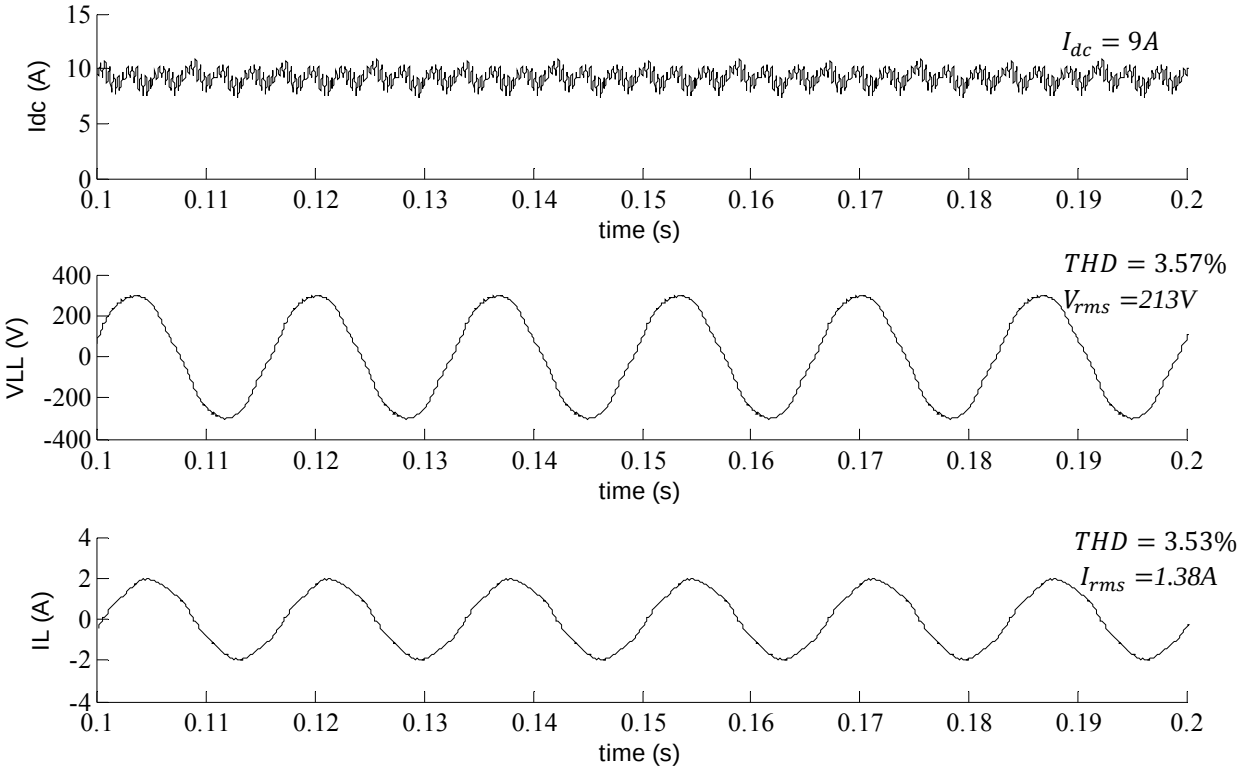


Figure 6-11 Simulation Results for V_{dc}=55V, C_{ac}=20µF and R_{load}=90Ω

6.3.3 Simulation Results for V_{dc}=60V

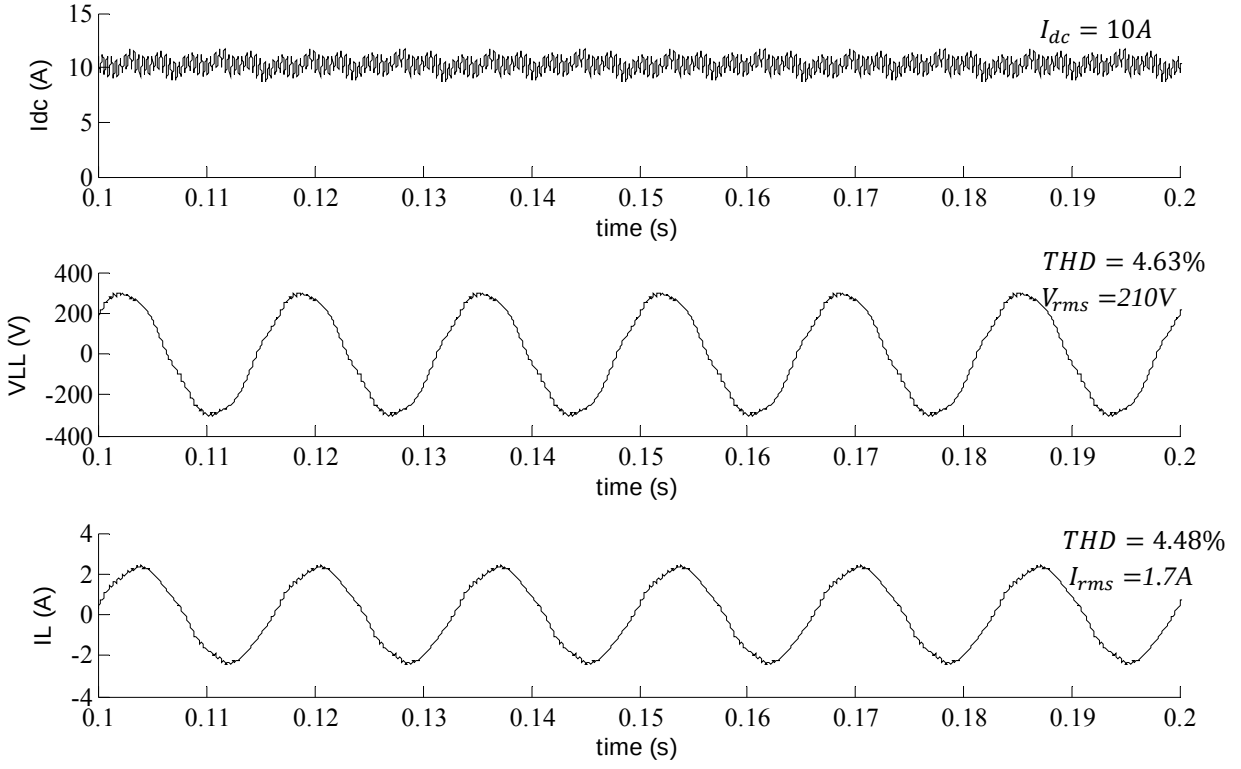


Figure 6-12 Simulation Results for V_{dc}=60V, C_{ac}=10µF and R_{load}=75Ω

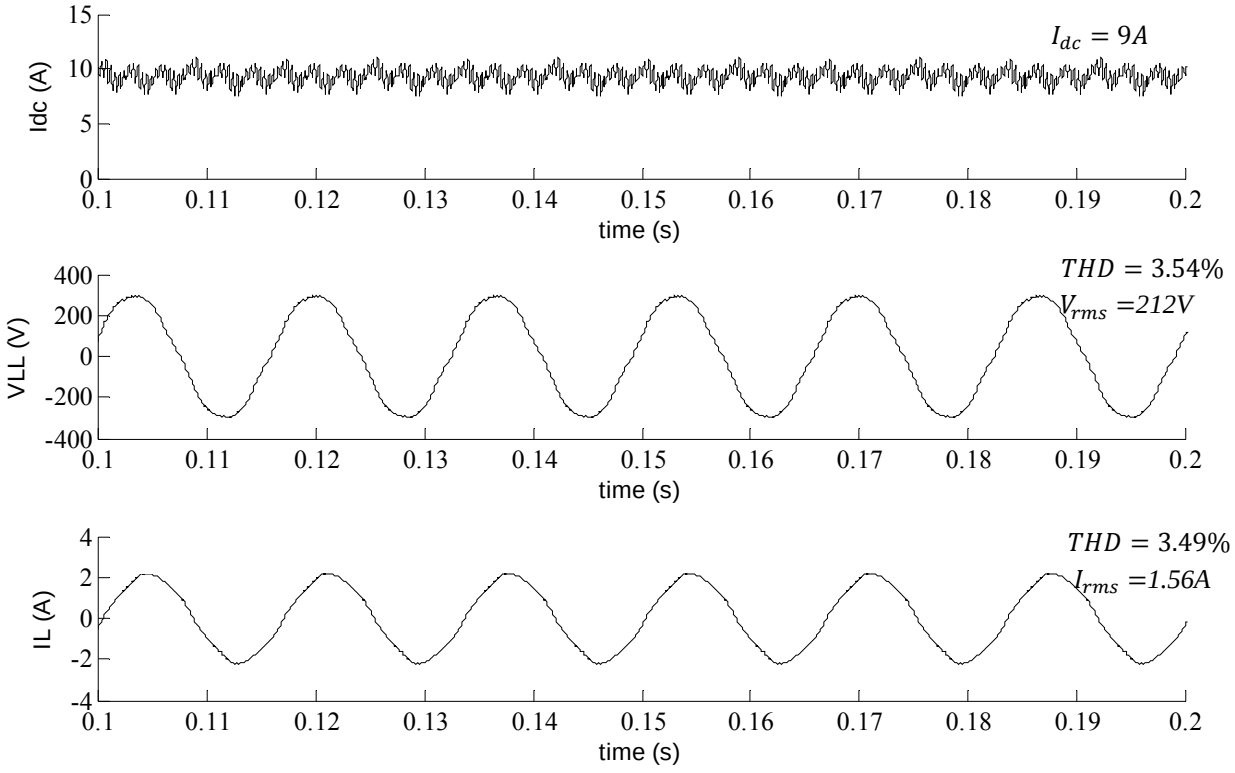


Figure 6-13 Simulation Results for V_{dc}=60V, C_{ac}=20µF and R_{load}=80Ω

6.3.4 Simulation Results for V_{dc}=65V

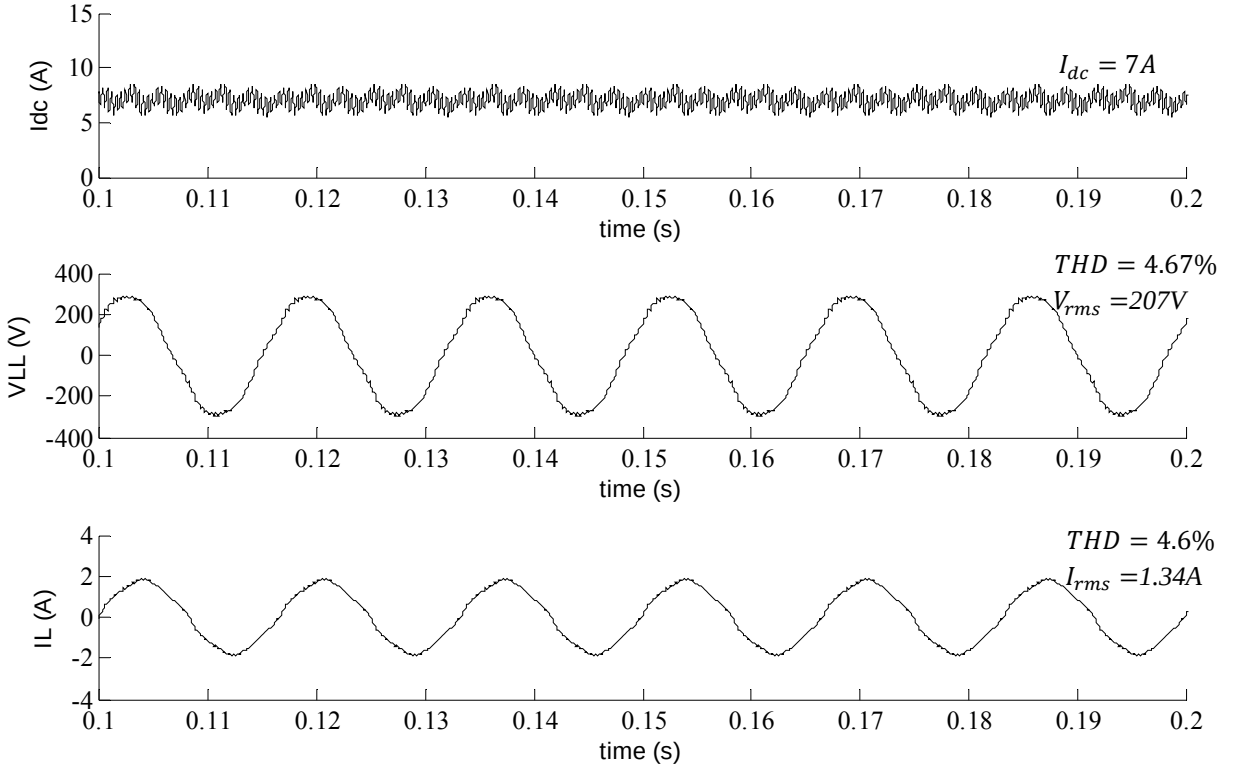


Figure 6-14 Simulation Results for V_{dc}=65V, C_{ac}=10µF and R_{load}=95Ω

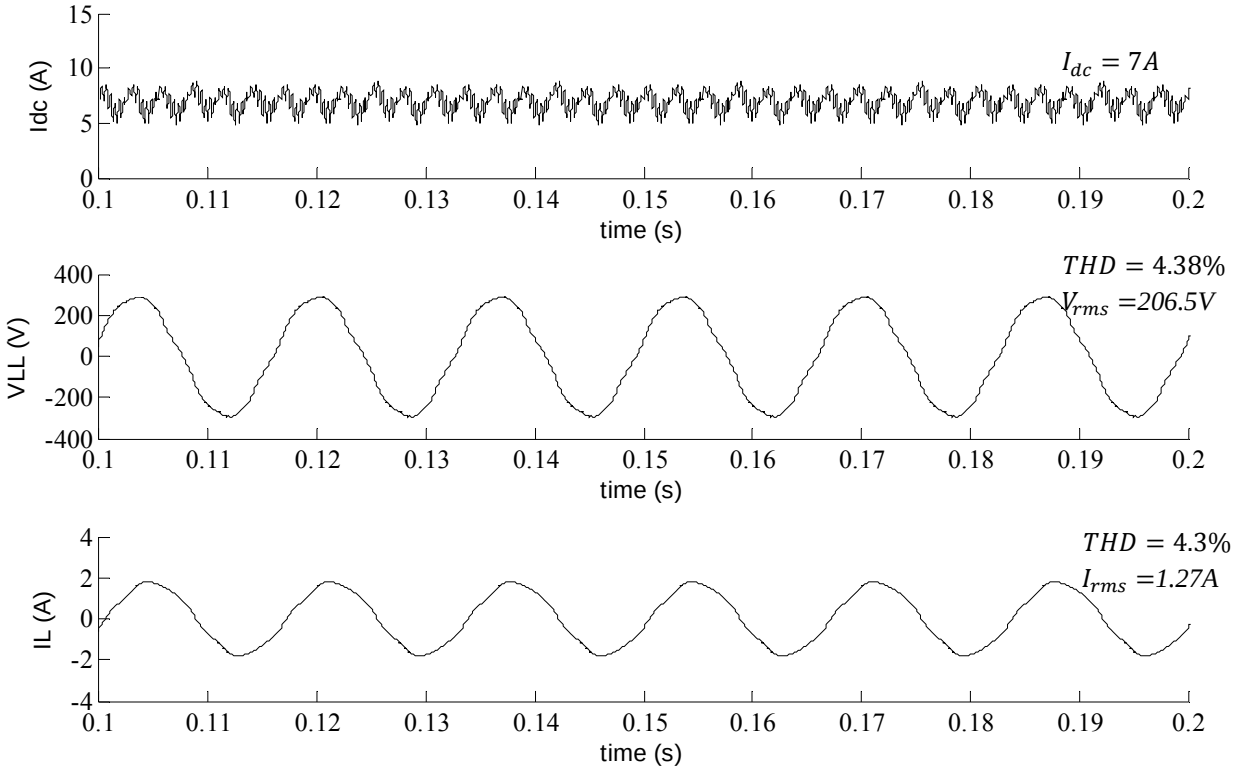


Figure 6-15 Simulation Results for V_{dc}=65V, C_{ac}=20µF and R_{load}=95Ω

6.3.5 Simulation Results for V_{dc}=70v

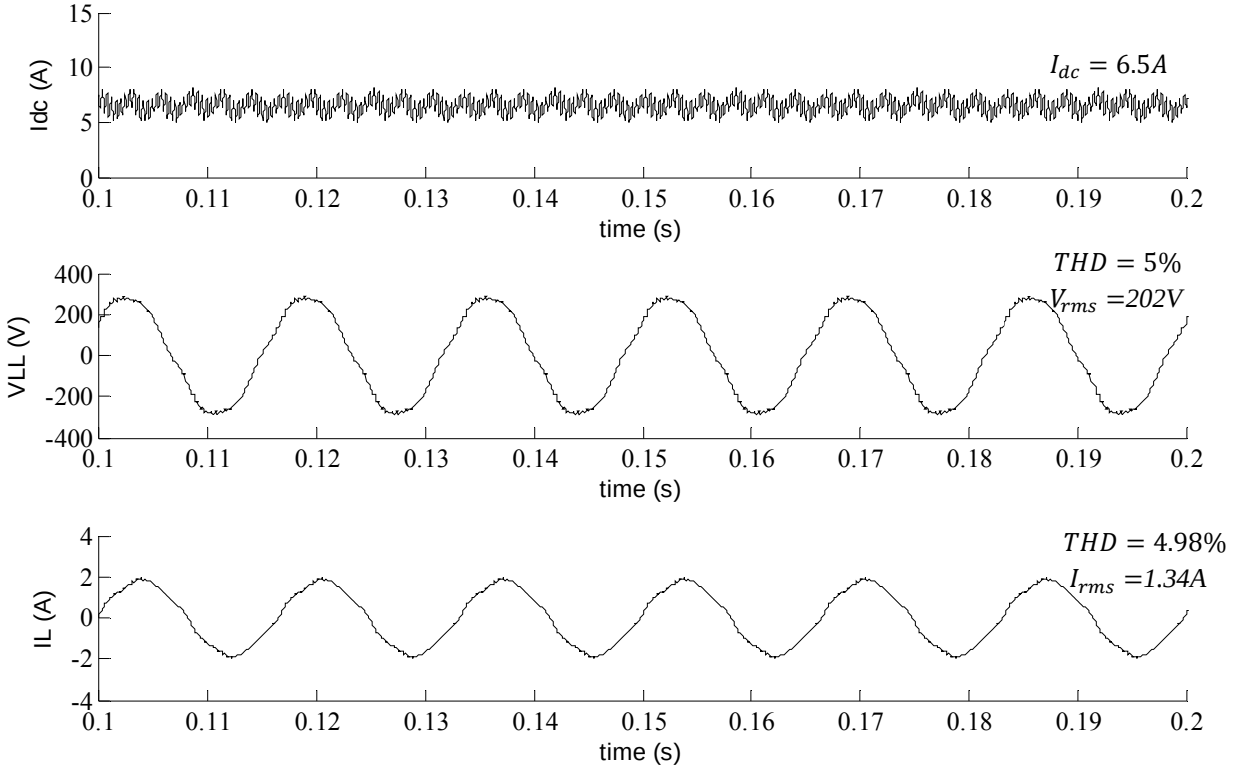


Figure 6-16 Simulation Results for V_{dc}=70V, C_{ac}=10µF and R_{load}=90Ω

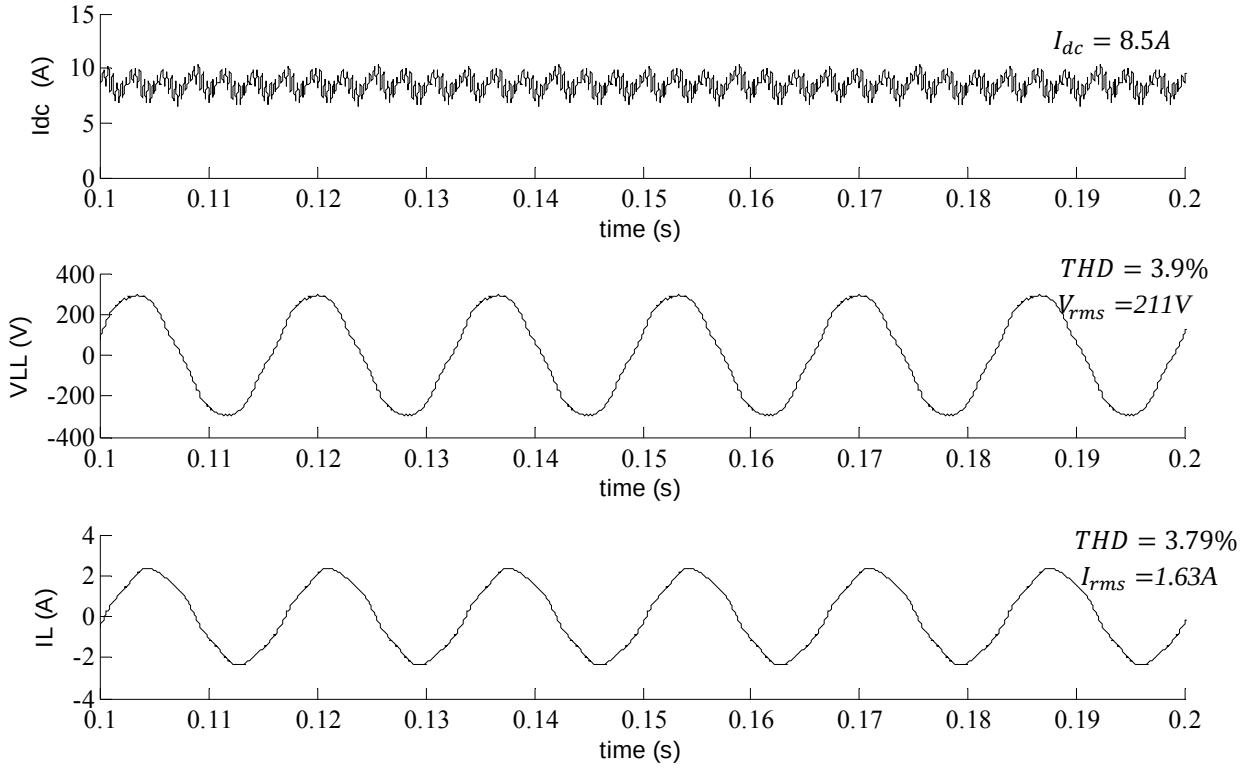


Figure 6-17 Simulation Results for V_{dc}=70V, C_{ac}=20µF and R_{load}=75Ω

6.3.6 Simulation Results for V_{dc}=75v

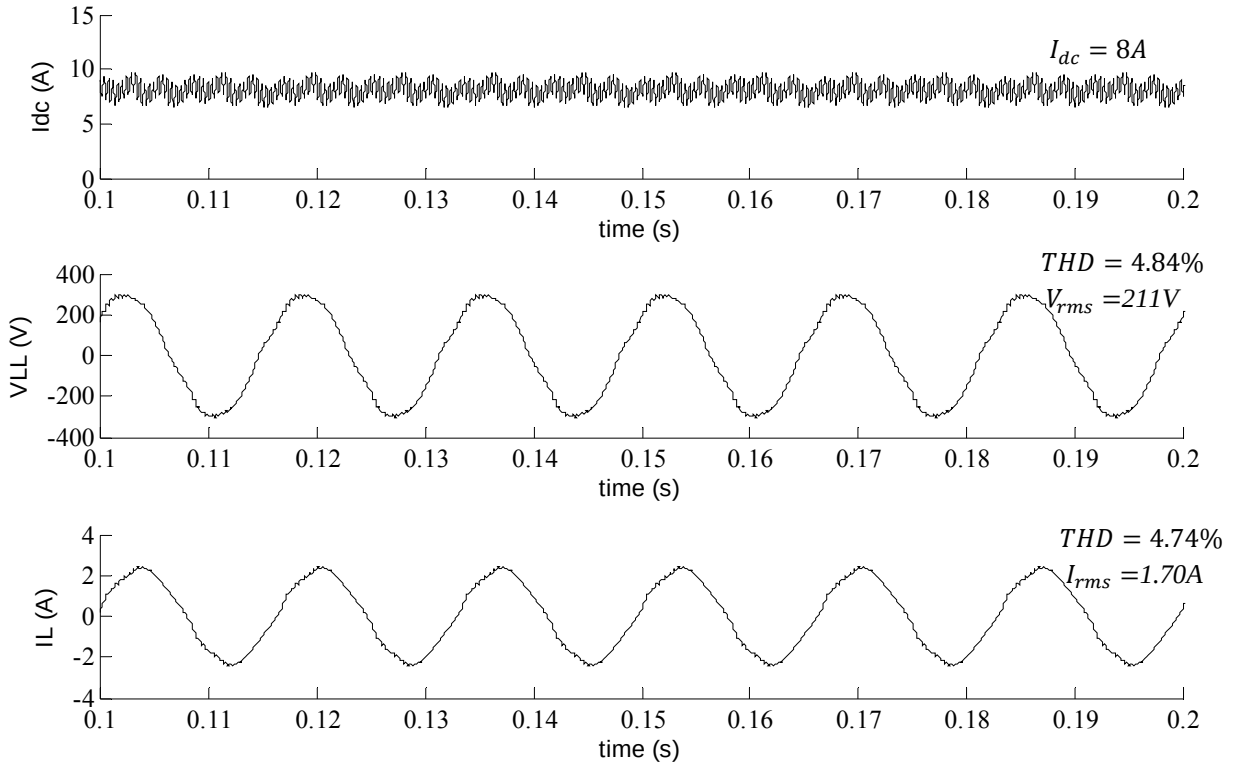


Figure 6-18 Simulation Results for V_{dc}=75V, C_{ac}=10µF and R_{load}=75Ω

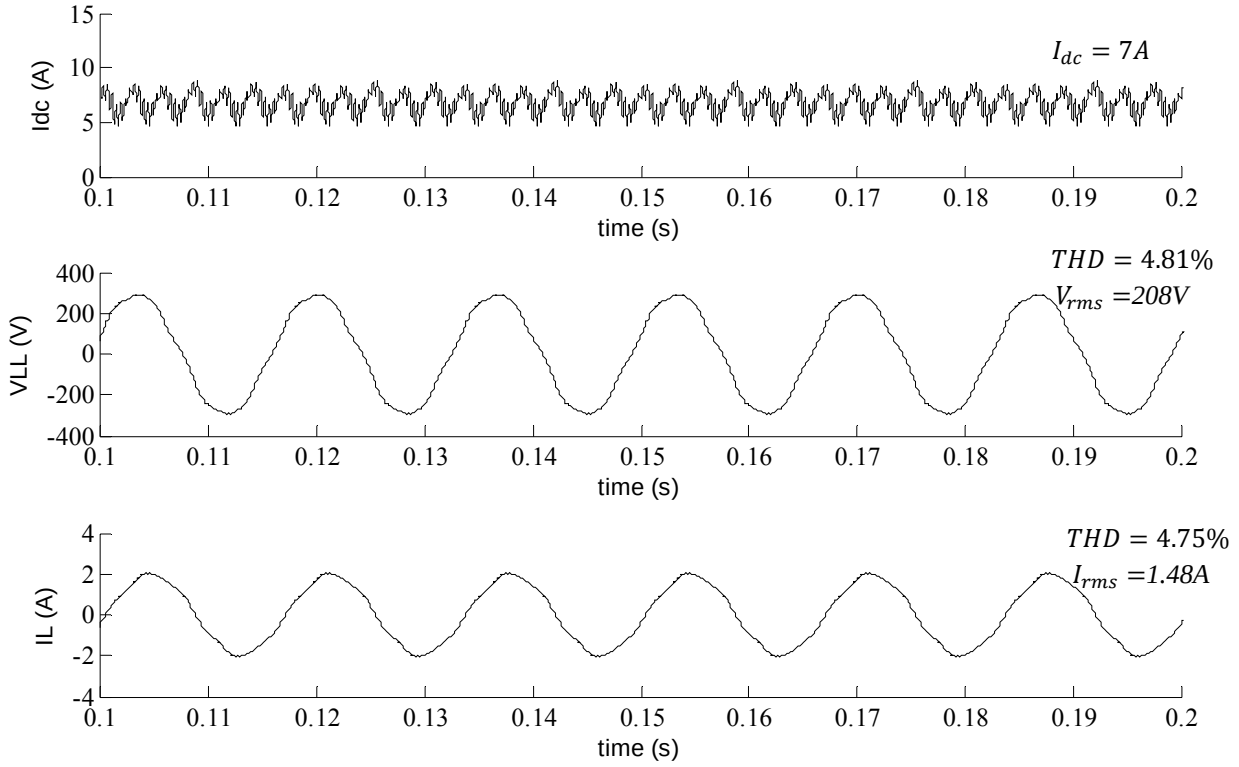


Figure 6-19 Simulation Results for V_{dc}=75V, C_{ac}=20µF and R_{load}=85Ω

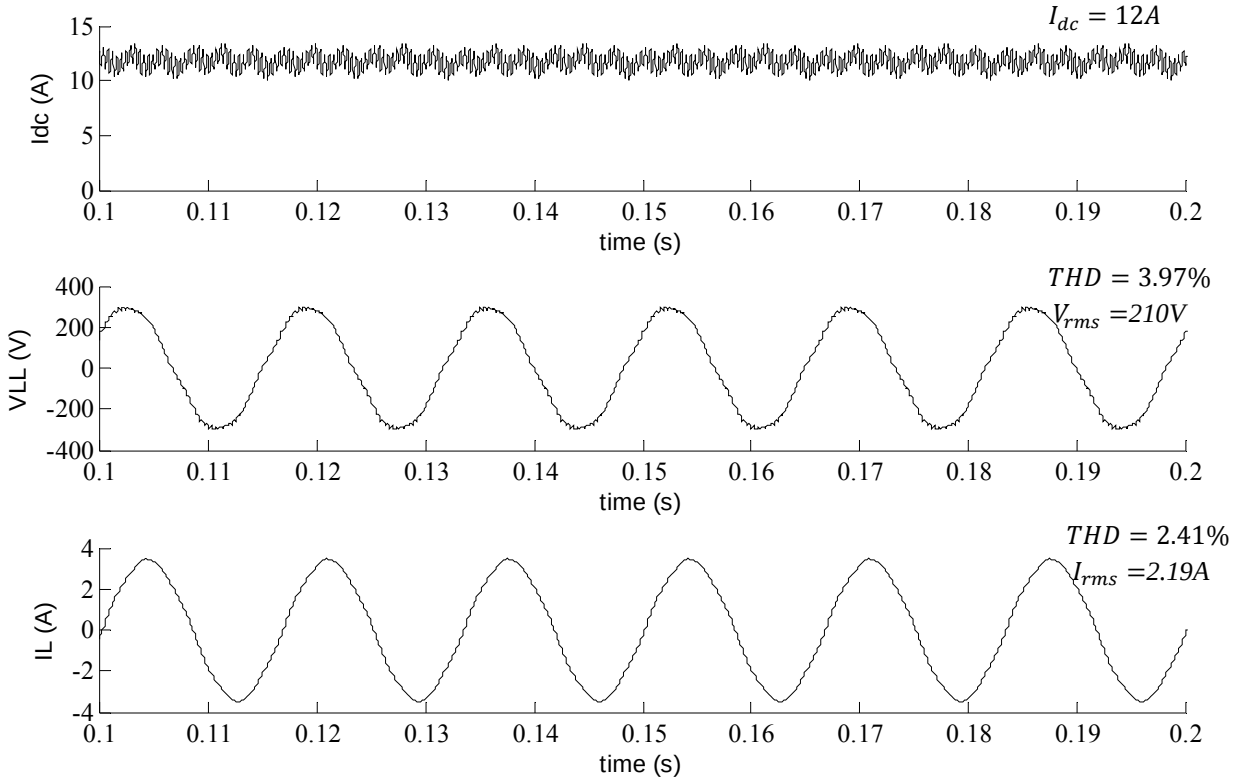


Figure 6-20 Simulation Results for V_{dc}=75V, C_{ac}=20µF, R_{load}=50Ω and L_{load}=17.5mH

6.3.7 Simulation Results for V_{dc}=80v

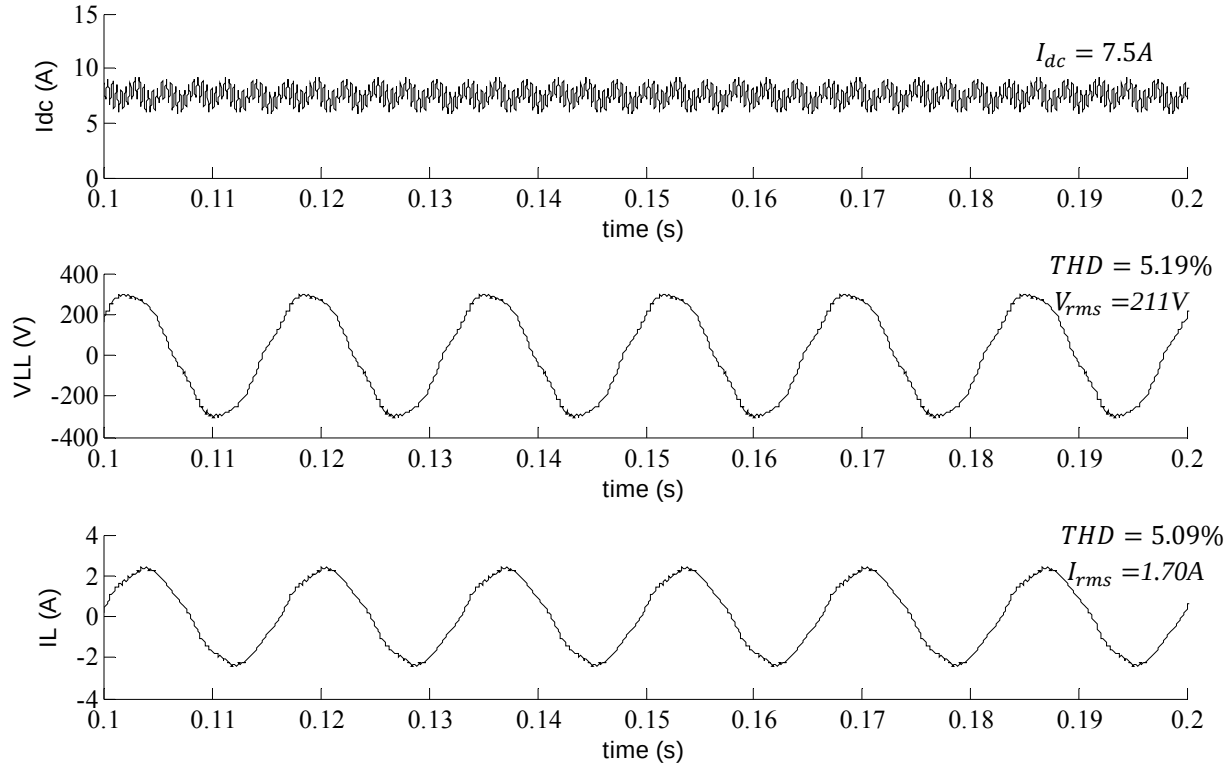


Figure 6-21 Simulation Results for V_{dc}=80V, C_{ac}=10µF and R_{load}=75Ω

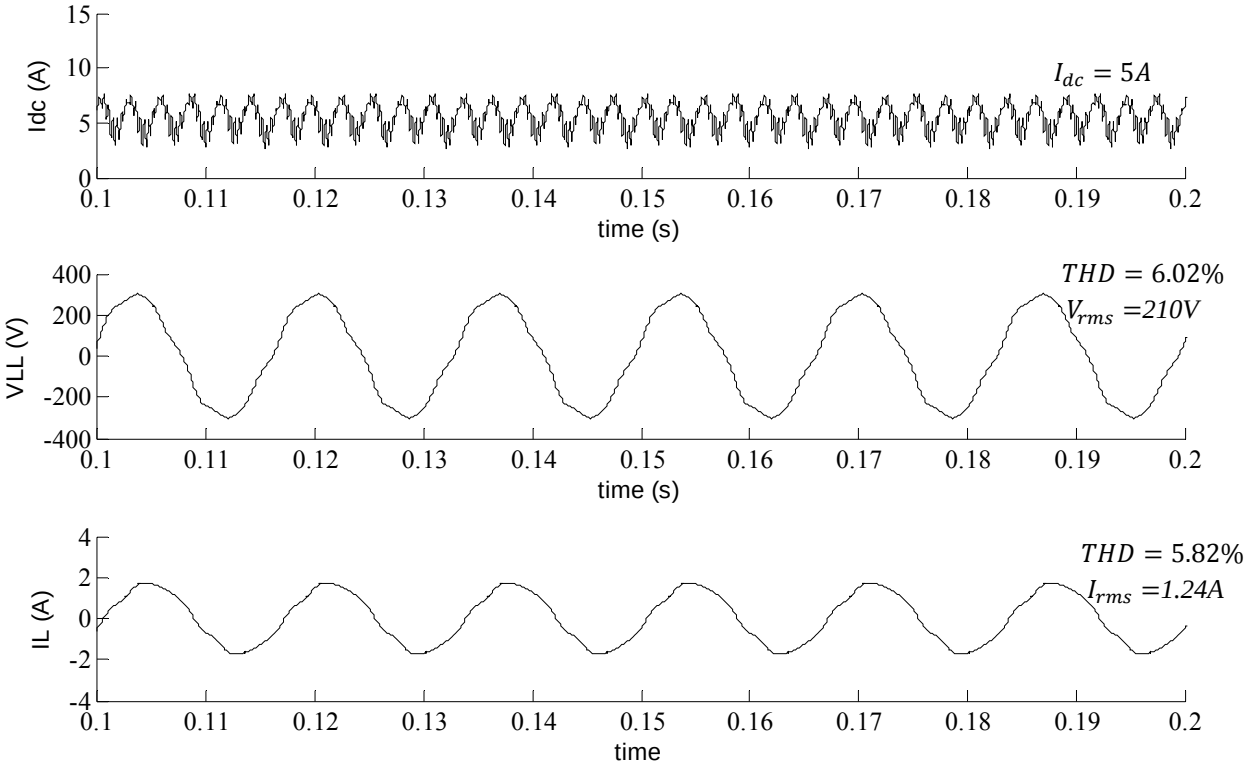


Figure 6-22 Simulation Results for V_{dc}=80V, C_{ac}=20µF and R_{load}=100Ω

6.4 Comparison between Simulink Results

In this section, results presented in the previous section are compared to each other. A comparison between Figure 6-7 and Figure 6-8 shows that in constant input DC voltage, increase in load decreased the DC current and rms (and peak) of line current. This can be explained by the fact that while the inverter is working in current-source voltage-regulated mode, increase in the load will decrease the current needed to regulate the voltage to the same level. Therefore, the charging ratio (D) will be less and the input current will decrease. Also, a comparison between Figure 6-7 and Figure 6-21 shows that increasing the input voltage while keeping the load and AC side capacitor constant will decrease the input current. This can be explained by saying that while the circuit is identical for both cases, the input power needed in two cases is almost the same. Therefore, increase in input DC voltage will decrease the input current needed to reach the desired output voltage. By comparing Figure 6-14 and Figure 6-15, it can be seen that increasing C_{ac} will reduce the charging ratio (D) needed and decrease THD.

6.5 Simulation Results using Higher Resolution Processor

As it was mentioned earlier, using a processor with a higher resolution will result in less distorted output waveforms.

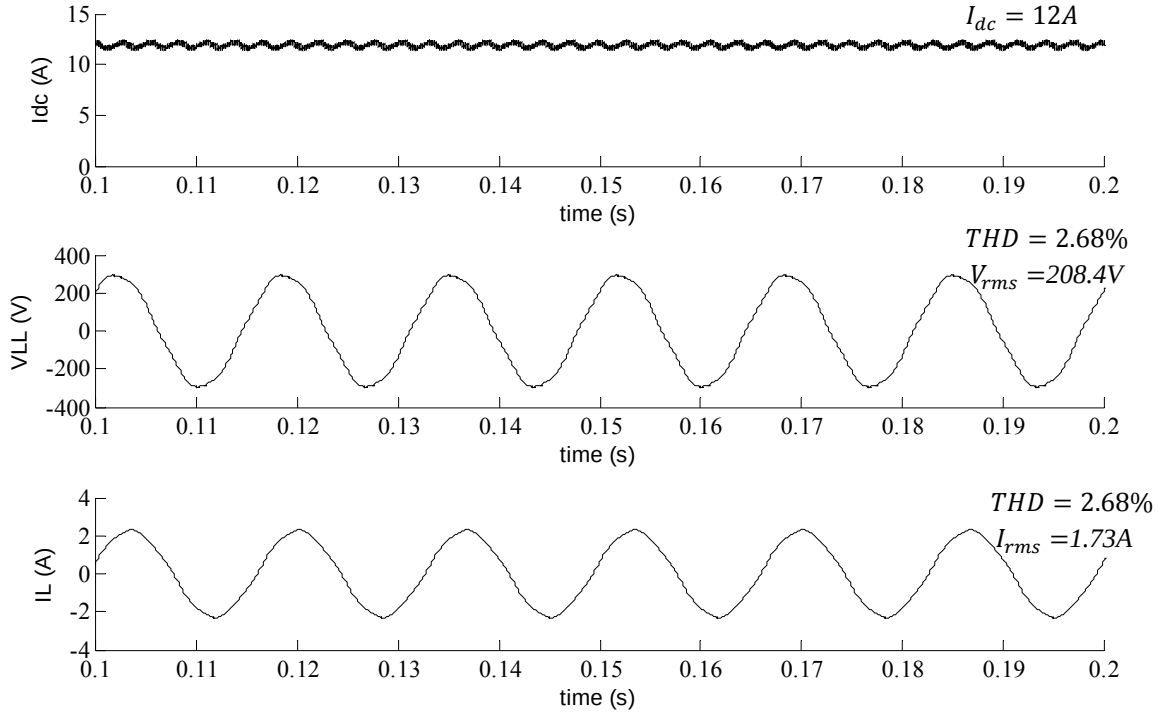


Figure 6-23 Simulation Results for V_{dc}=50V, C_{ac}=10μF and R_{load}=75Ω with a Higher Resolution Processor (f_{sw}=7.2 kHz)

Figure 6-23 shows simulation results for the same circuit configuration as Figure 6-7 with the difference of changing the step size to 0.1 times the previous case. In this case, it has been assumed that the switching frequency is 7.2 kHz and the total number of points in every switching cycle is 100. Comparison of Figure 6-7 and 6-23 shows that reducing the step size has significantly improved the performance of the system. FFT analysis of the output current is shown in Figure 6-24.

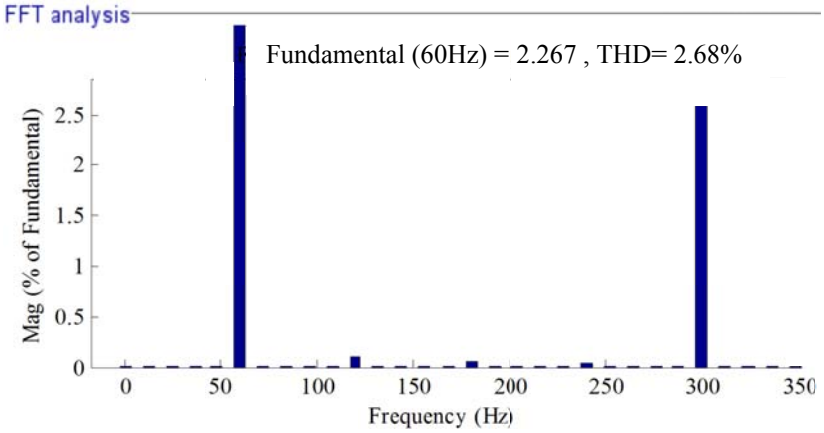


Figure 6-24 FFT Analysis of the Line Current for V_{dc}=50V, C_{ac}=10μF and R_{load}=75Ω with a Higher Resolution Processor

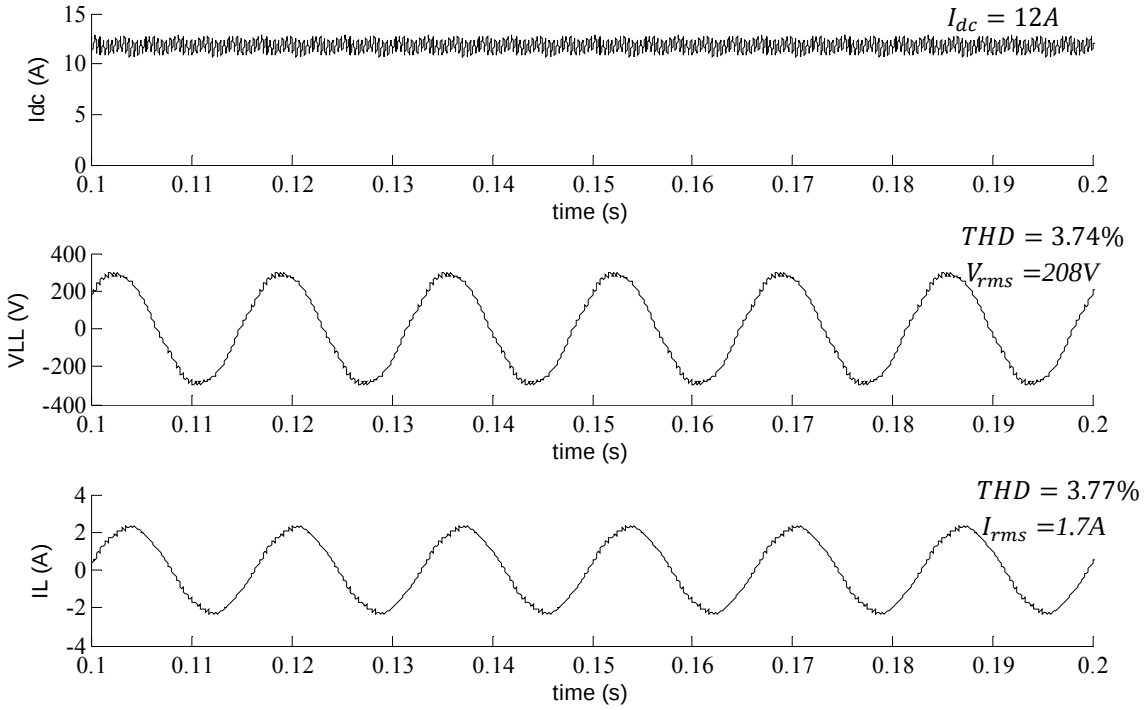


Figure 6-25 Simulation Results for V_{dc}=50V, C_{ac}=10μF and R_{load}=75Ω with a Higher Resolution Processor (f_{sw}=2.4 kHz)

If the switching frequency of the system is kept at 2.4 kHz but the number of points in every switching cycle is increased to 300 points (thus the step size which is $\frac{1}{N_{total}*f_{sw}}$ is still 0.1 times the previous case), results in Figure 6-25 show that the desired output line to line voltage can be achieved with THD of less than 5%.

As shown in the above figures, using a higher resolution processor for generating switching patterns will excessively help reduce the distortions in the output waveforms of the inverter.

6.6 Comparison between the New Proposed and Previous Method

In this section, results of the new proposed method and phasor pulse width modulation method (PPWM) are compared to each other. Previously, in Figures 5-5, 5-6 and 5-11, it was demonstrated that the advantage of using the new proposed method over the old method is that the new method makes the switching pattern symmetric in some parts which will reduce the distortions in the output signal. Figure 6-26 shows simulation results for DC link current, line to line voltage, and line current of the boost inverter using the old method for V_{dc}=80V, C_{ac}=10µF and load=90Ω. FFT analysis of line to line voltage is given in Figure 6-27. Figure 6-28 and 6-29 show the same information using the new proposed method. As seen in the following figures, total harmonic distortion has been decreased using the new proposed method.

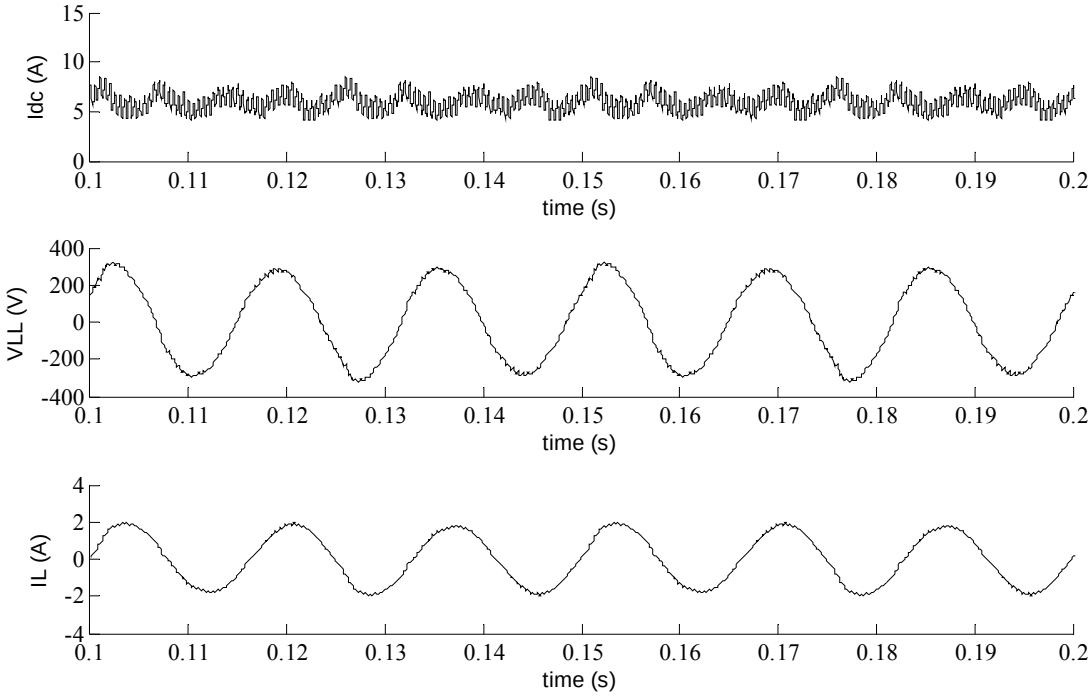


Figure 6-26 Simulation Results for V_{dc}=80V, C_{ac}=10µF and R_{load}=90Ω Using PPWM Method

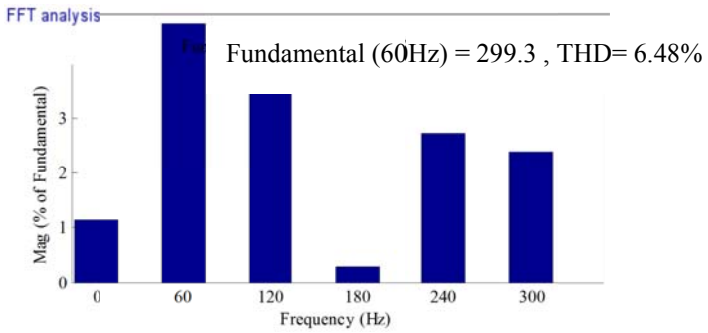


Figure 6-27 FFT Analysis of the Line to Line Voltage for V_{dc}=80V, C_{ac}=10µF and R_{load}=90Ω Using PPWM Method

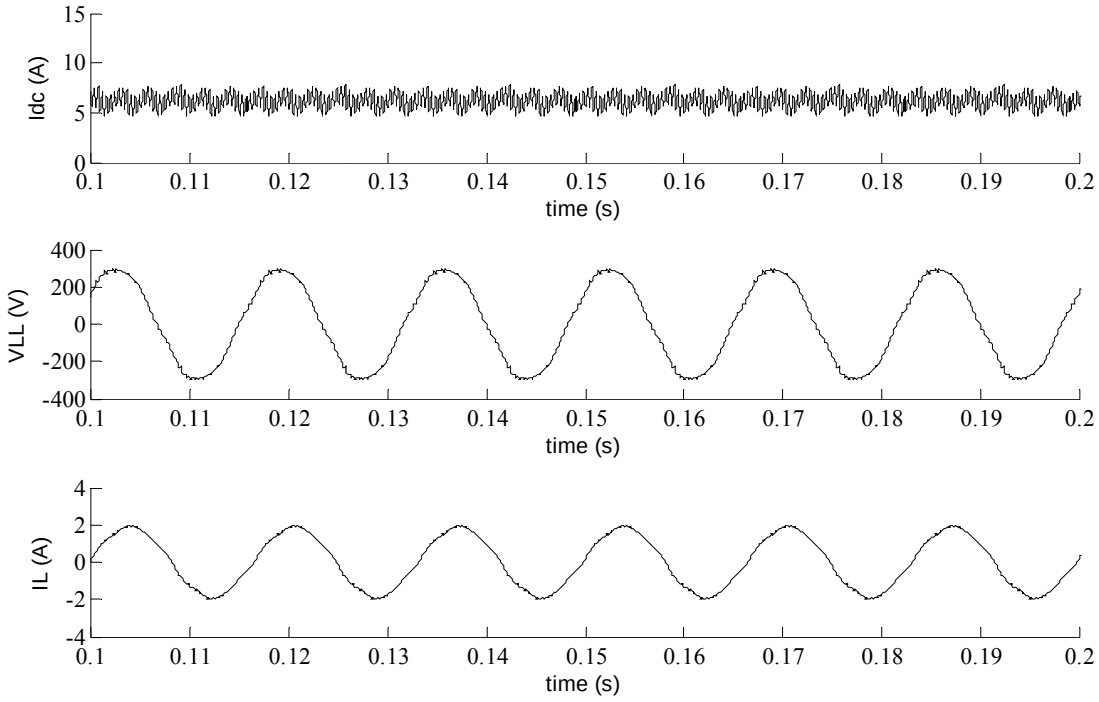


Figure 6-28 Simulation Results for V_{dc}=80V, C_{ac}=10µF and R_{load}=90Ω Using Modified PPWM Method

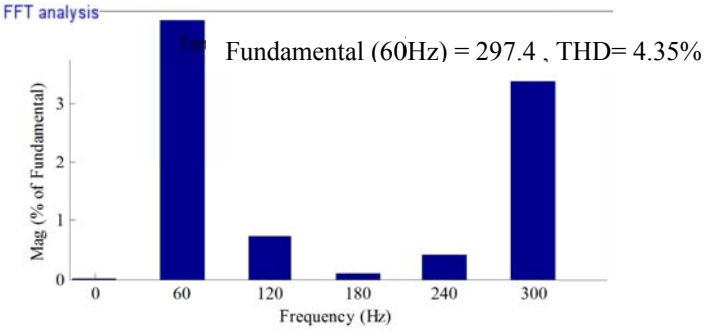


Figure 6-29 FFT Analysis of the Line to Line Voltage for V_{dc}=80v, C_{ac}=10µF and R_{load}=90Ω Using Modified PPWM Method

6.7 Conclusion

In this chapter, a Simulink model was developed to apply the modified phasor pulse width modulation to a boost inverter. Blocks used for generating the switching pattern, output voltage control and inverter design were explained in detail. Simulation results for different input voltages, loads and AC-side capacitors were given and the results were compared to each other. Moreover, simulation results using a higher resolution processor were given which showed that increase in the resolution of the system will improve the performance of the system. At the end of the chapter, a comparison between the results of applying PPWM and modified PPWM methods to the boost inverter was given which demonstrated that using modified PPWM method will decrease distortions in the output voltage/current waveform of the system.

Chapter 7 - Experimental Results

7.1 Introduction

In this chapter, experimental results of the application of the modified phasor pulse width modulation to a boost inverter are presented. Printed circuit board of a laboratory-scaled current source inverter was designed using Cadence software. A scene of the experimental setup has been shown in Figure 7-1. Table 7-1 provides some information about circuit components, and Table 7-2 offers the values of these components. The inverter was run for several circuit component sets and loads, and the results are presented for each case.

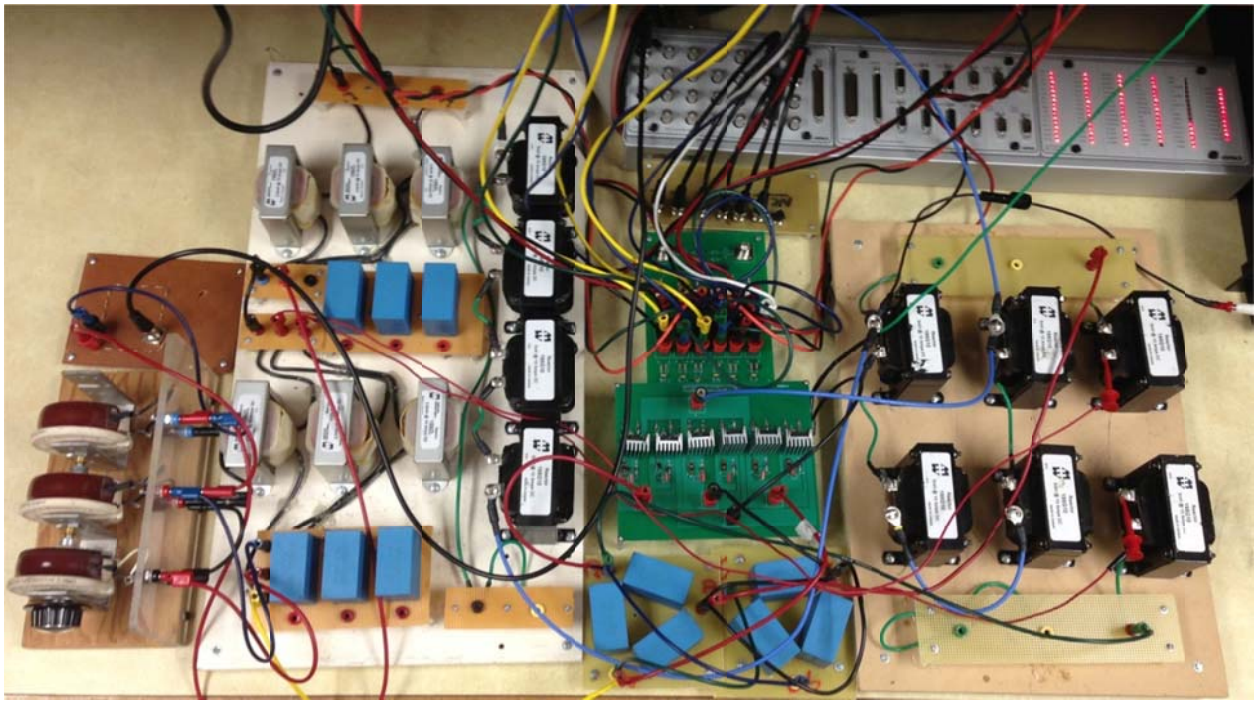


Figure 7-1 Experimental Prototype

Table 7-1 Specifications of The Experimental Setup

Signal Generator	CP1103 dSPACE
Input DC Source	Agilent technologies (N5768A)
DC Power Supply	BK Precision 1761
Measurement	LeCroy Waverunner 64XI-A oscilloscope
Probe	ADP305 differential voltage probe CP030 current probe
IGBT Switch	IXRH 25N120
Optocoupler	Fairchild 3120 (1039B)
Inductor	Hammond Manufacturing

Table 7-2 Experimental Circuit Component Values and Data

Input DC Voltage	50-80 volts
L_{dc}	10mH
C_{ac}	10μF & 20μF
L_{filter}	7.5mH
Load	Resistive Load: 75-100Ω Resistive Inductive Load: R_L=50Ω & L_L=20mH
f_{sw}	2.4kHz
N_{total}	41

7.2 Simulink Model Modification

While the dSPACE system used in this experiment has a limited step size of 10μs, the frequency and total number of points in every switching cycle (explained in chapter 4) is limited. While the difference between two consecutive sample points should be more than the system step size, the switching frequency was chosen to be 2.4kHz and the total number of sample points in every switching cycle was chosen to be 41. In this case, difference between two consecutive points is $\frac{1}{2400*41} \simeq 10.1626\mu s$ which is higher than the minimum step size that can be used.

Also, a path for the current of the DC-side inductor should always be guaranteed. While the experimental system is not an ideal system (step size is limited), there is a possibility that in a switching cycle, when the system is changing from charging state to a discharging state or is changing from a discharging state to another discharging state, arrangement of the switches makes an open circuit across the inductor for a short period of time. Therefore, no path will be present for the inductor current, and this will produce a huge voltage ($L\frac{di}{dt}$) across the switches which will burn the switches. In order to solve this problem, the switching pattern has changed, slightly. In every switching cycle, for the first n_c points, the system is charging as before. After the charging state, for one point, switches of charging state and the switch needed for first discharging state (total of 3 switches) are 'ON'. After this point, the extra switch becomes 'OFF'. Also, after the first discharging state, for one point, switches of first discharging state and the switch needed for second discharging state (total of 3 switches) are 'ON'. After this point, the extra switch becomes 'OFF'. This process is repeated in every switching cycle. For example, the switching pattern in sector I becomes as follows:

Sector I:

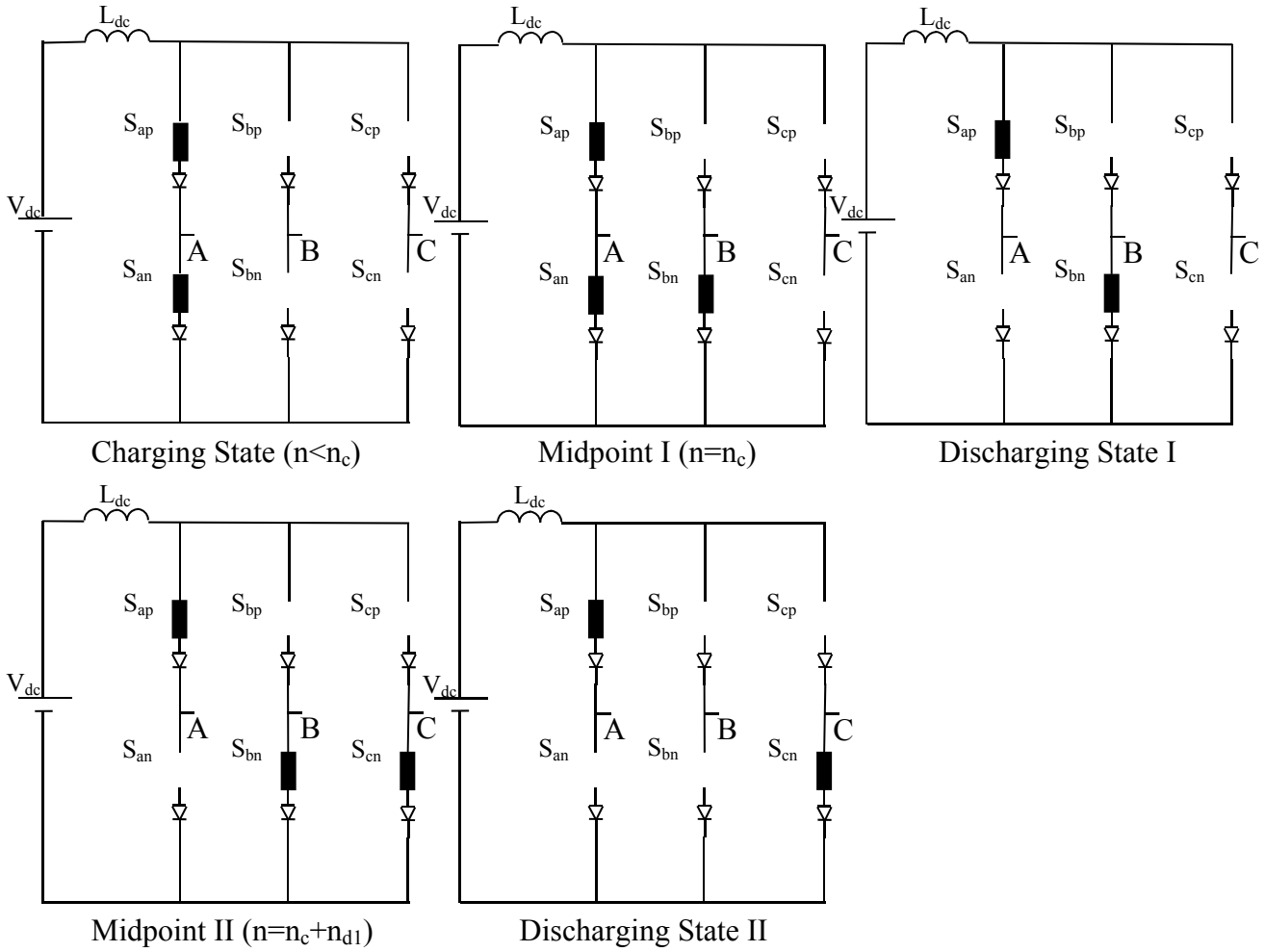


Figure 7-2 Modified Switching Pattern for Experimental Setup in Sector I

7.3 Experimental Results

7.3.1 DC Link Inductor Voltage and Current

Voltage across the DC link inductor and the current passing through it was measured when the input voltage was 75V, C_{ac} is 20μF, and the load is a resistive-inductive load of R_L=50Ω & L_L=17.5mH. Results are shown in Figure 7-3. Moreover, Figure 7-4 shows an expanded view of these waveforms. The top figure shows voltage across the inductor, and the bottom figure shows the current passing through the inductor. Results are consistent with the information in Figure 5-4.

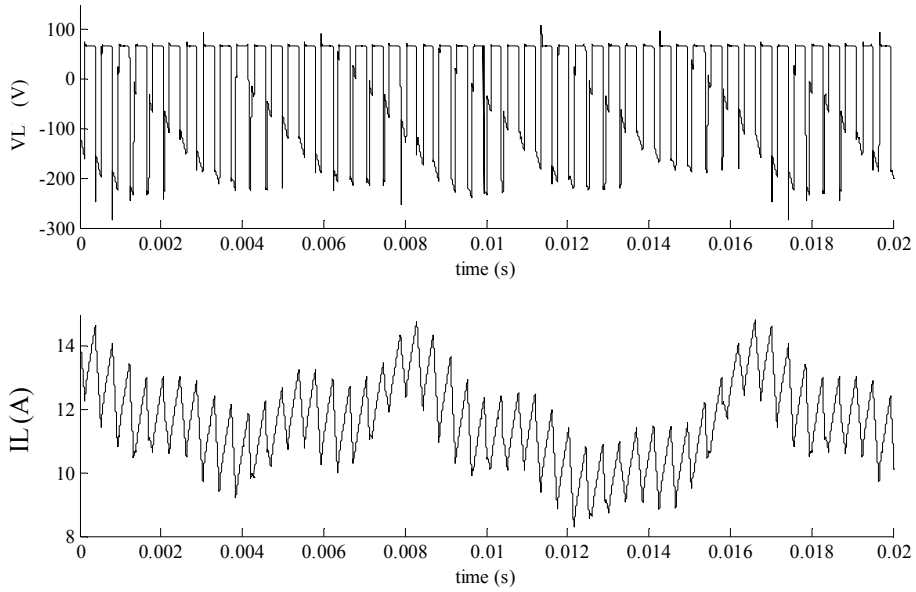


Figure 7-3 Inductor Voltage and Current Waveforms for V_{dc}=75V, C_{ac}=20µF, R_L=50Ω & L_L=17.5mH

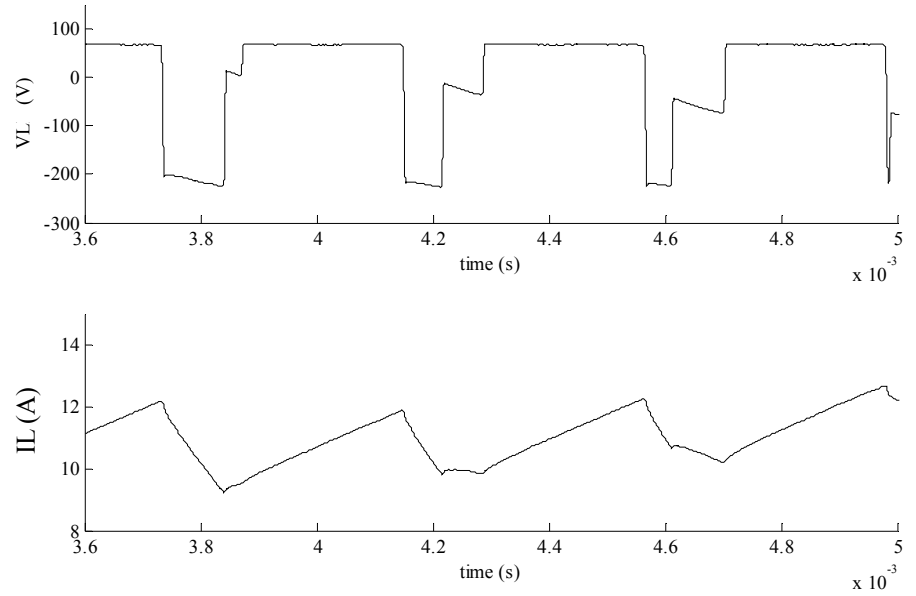


Figure 7-4 Expanded Inductor Voltage and Current Waveforms for V_{dc}=75V, C_{ac}=20µF, R_L=50Ω & L_L=17.5mH

In the next subsections, results of testing the circuit with different input DC voltages and loads are presented. In each figure, the first plot shows the output line to line voltage, the second plot shows the output line current, and the third plot shows the DC current.

7.3.2 Experimental Results for V_{dc}=50V

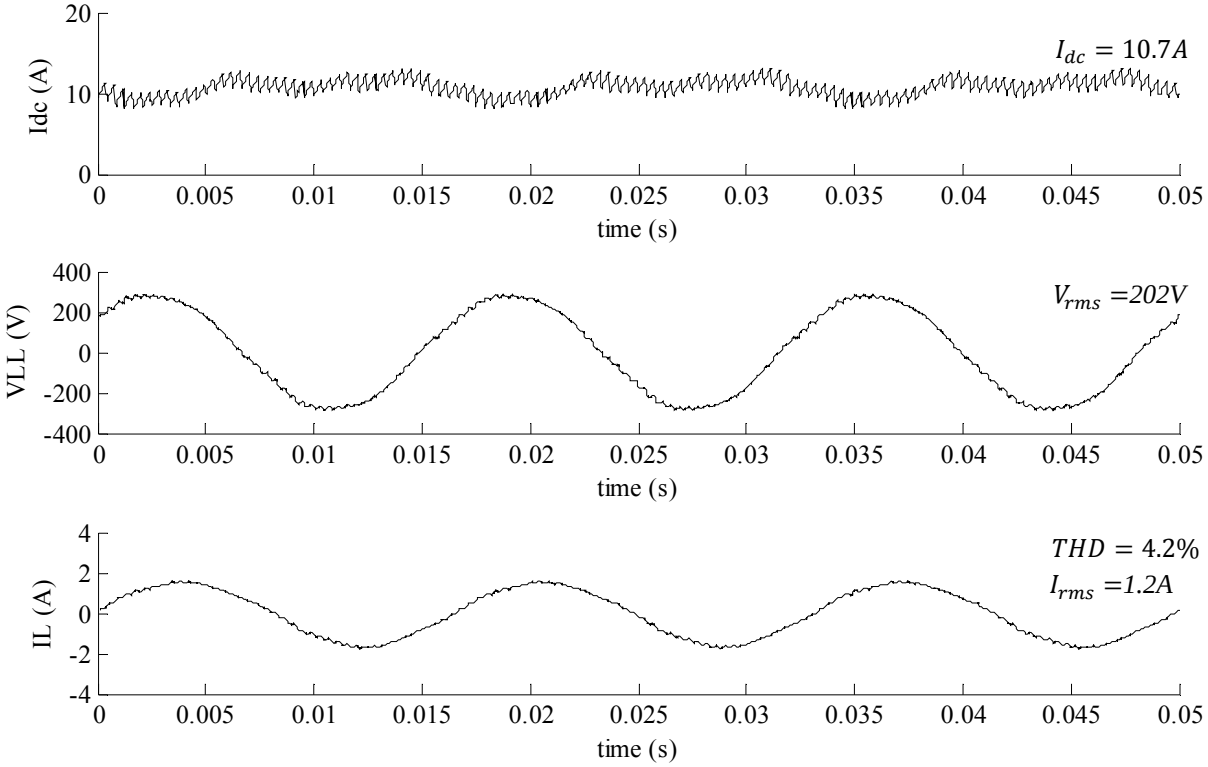


Figure 7-5 Experimental Results for V_{dc}=50V, C_{ac}=10µF and R_{load}=100Ω

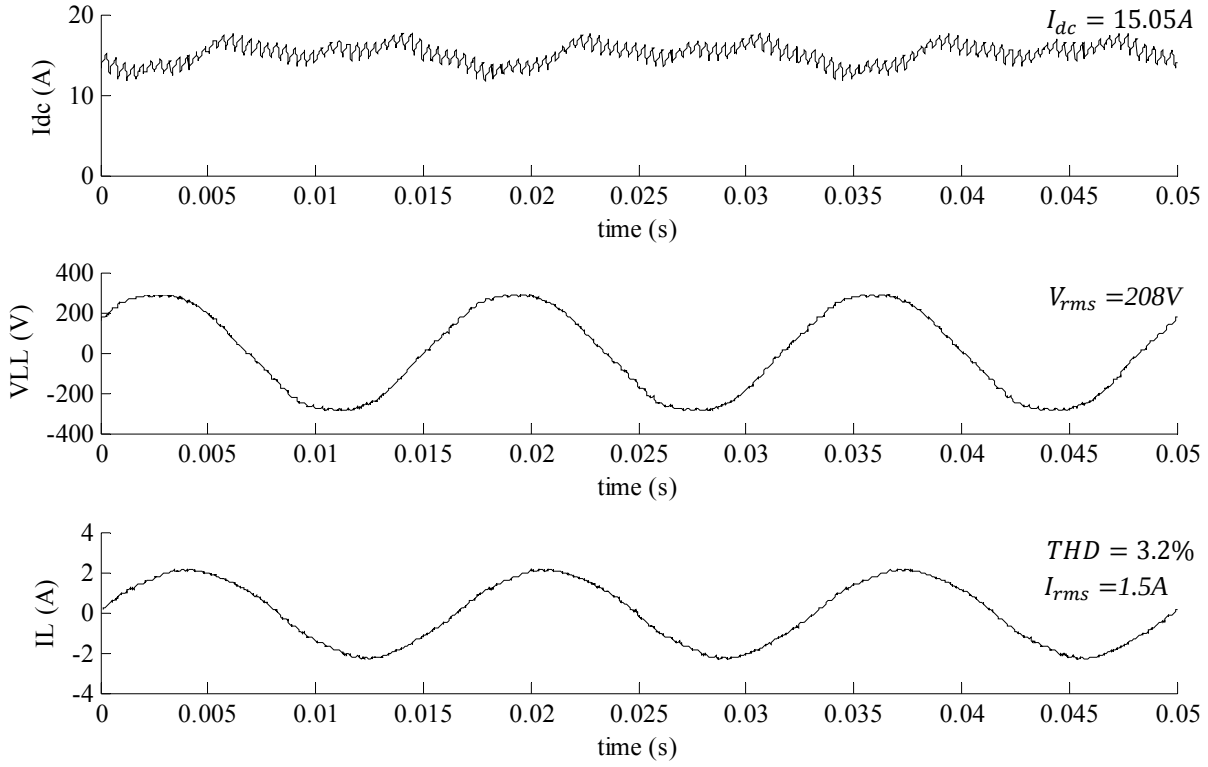


Figure 7-6 Experimental Results for V_{dc}=50V, C_{ac}=20µF and R_{load}=75Ω

7.3.3 Experimental Results for V_{dc}=55V

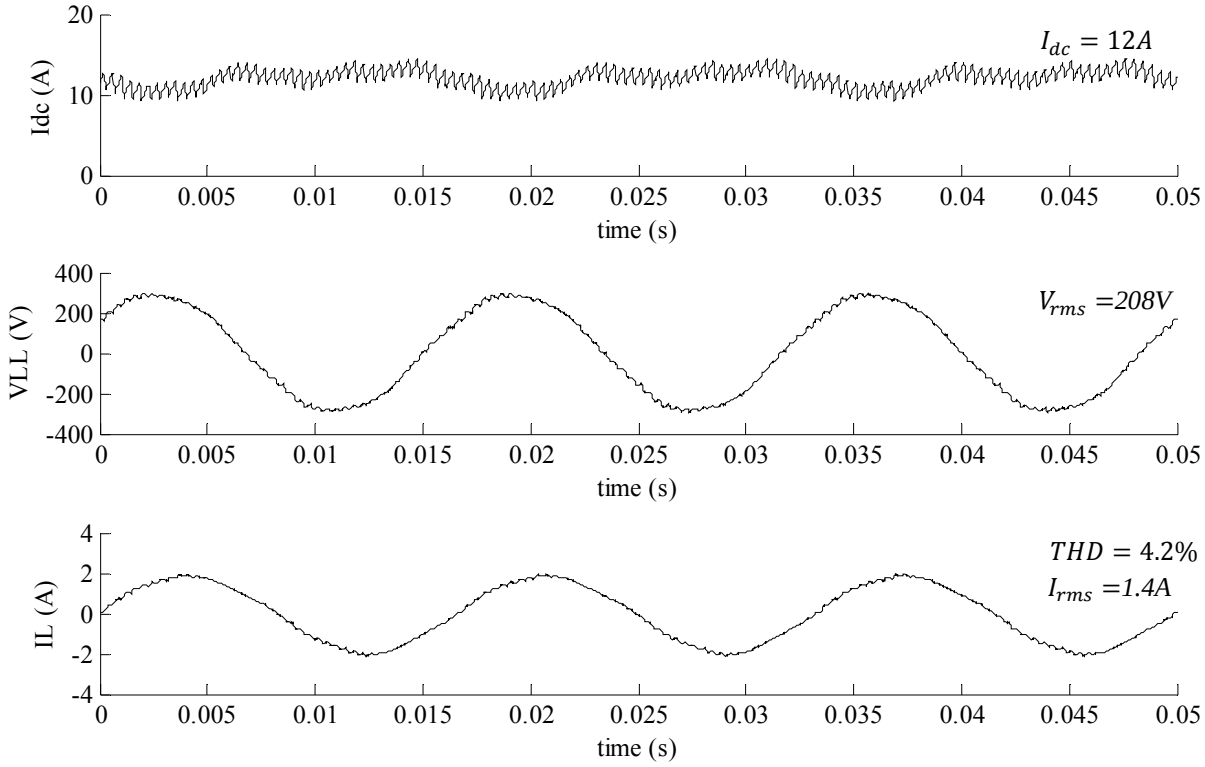


Figure 7-7 Experimental Results for V_{dc}=55V, C_{ac}=10µF and R_{load}=85Ω

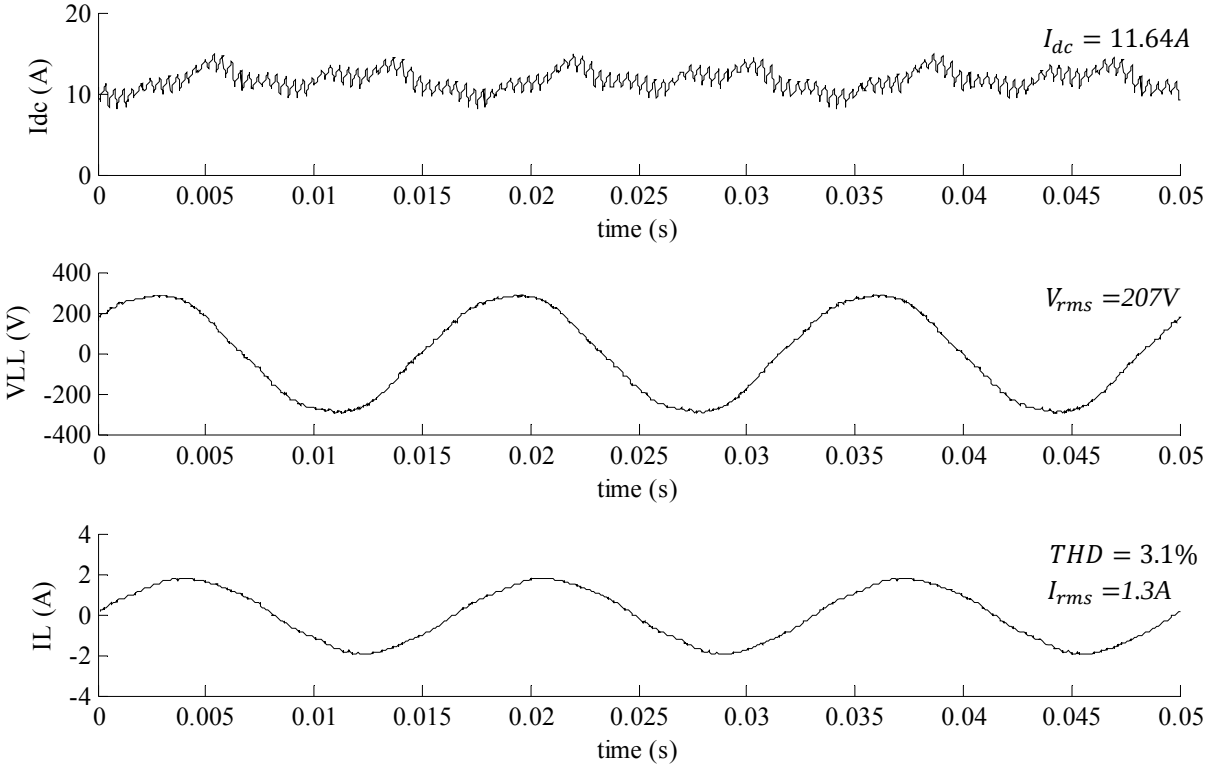


Figure 7-8 Experimental Results for V_{dc}=55V, C_{ac}=20µF and R_{load}=90Ω

7.3.4 Experimental Results for V_{dc}=60V

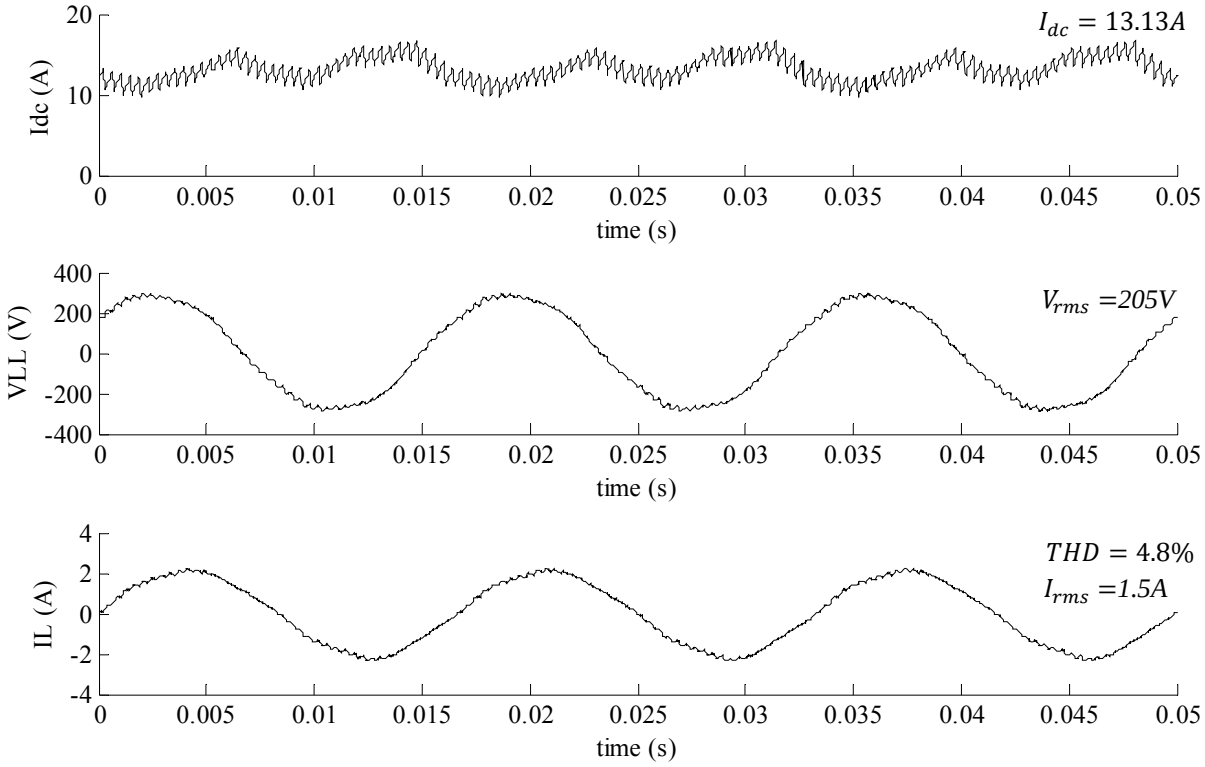


Figure 7-9 Experimental Results for V_{dc}=60V, C_{ac}=10µF and R_{load}=75Ω

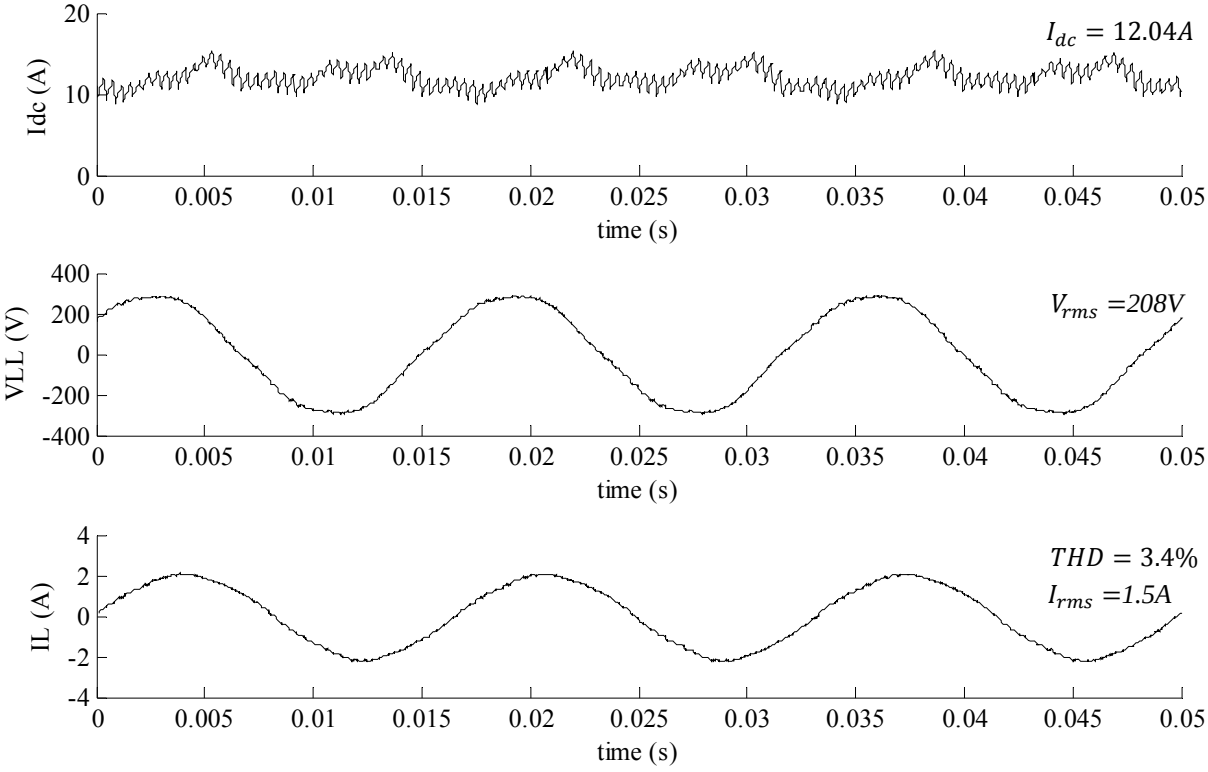


Figure 7-10 Experimental Results for V_{dc}=60V, C_{ac}=20µF and R_{load}=80Ω

7.3.5 Experimental Results for V_{dc}=65V

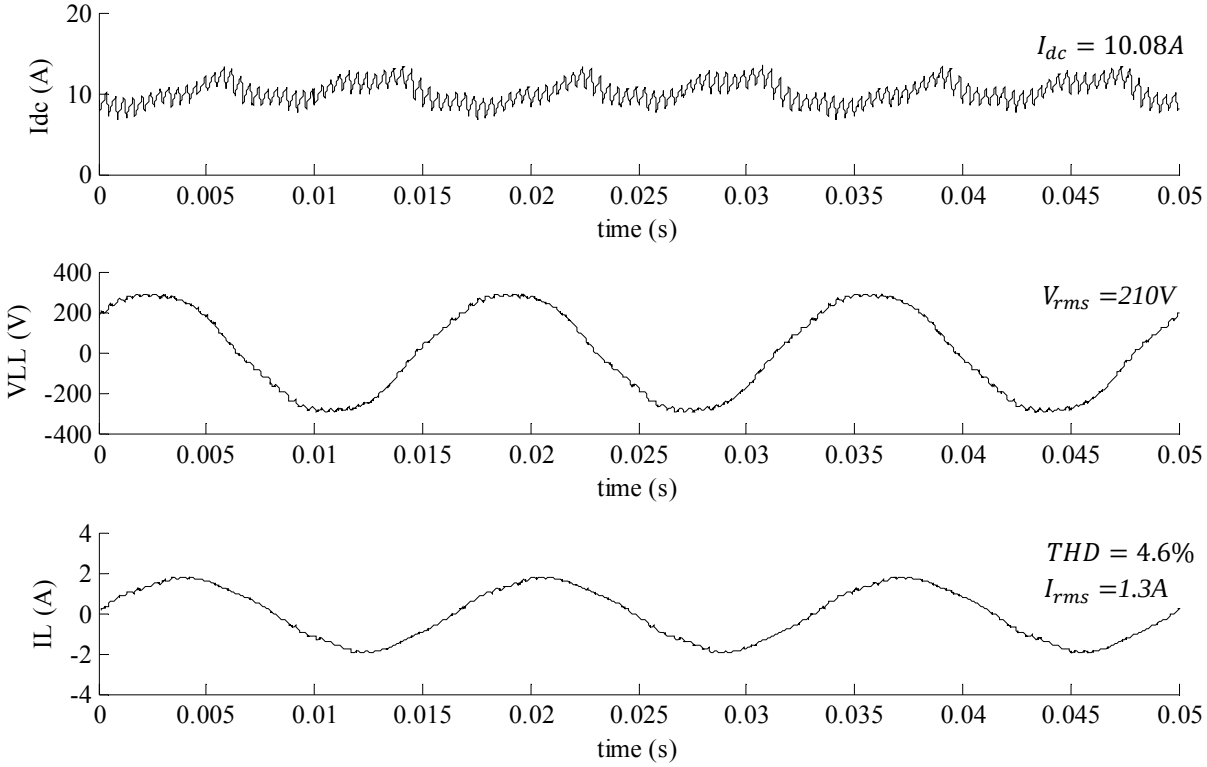


Figure 7-11 Experimental Results for V_{dc}=65V, C_{ac}=10µF and R_{load}=95Ω

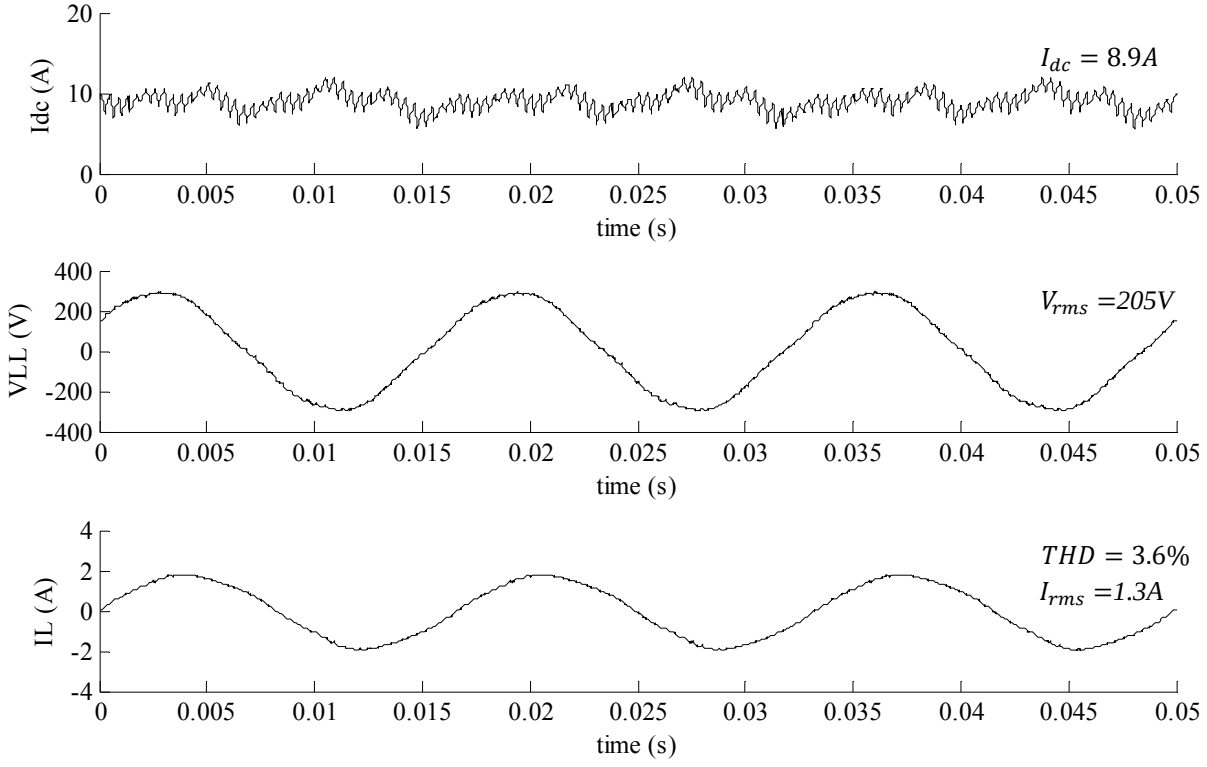


Figure 7-12 Experimental Results for V_{dc}=65V, C_{ac}=20µF and R_{load}=95Ω

7.3.6 Experimental Results for V_{dc}=70V

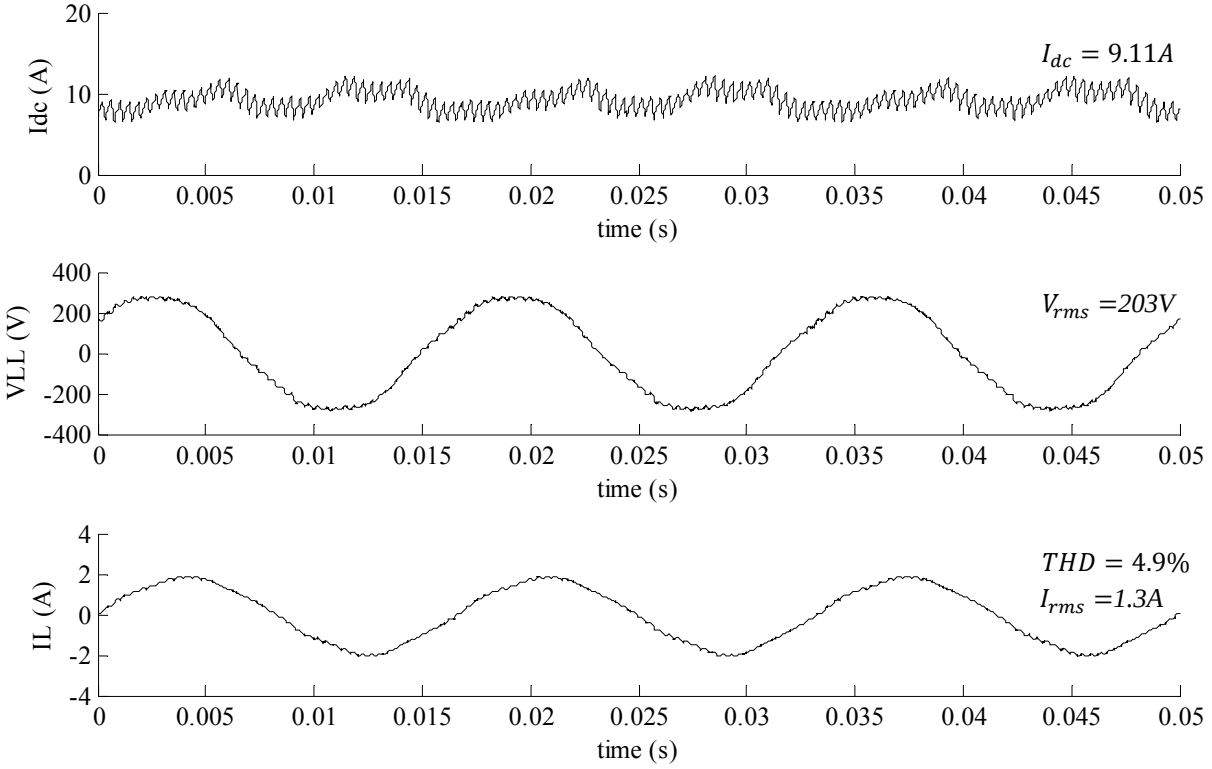


Figure 7-13 Experimental Results for V_{dc}=70V, C_{ac}=10µF and R_{load}=90Ω

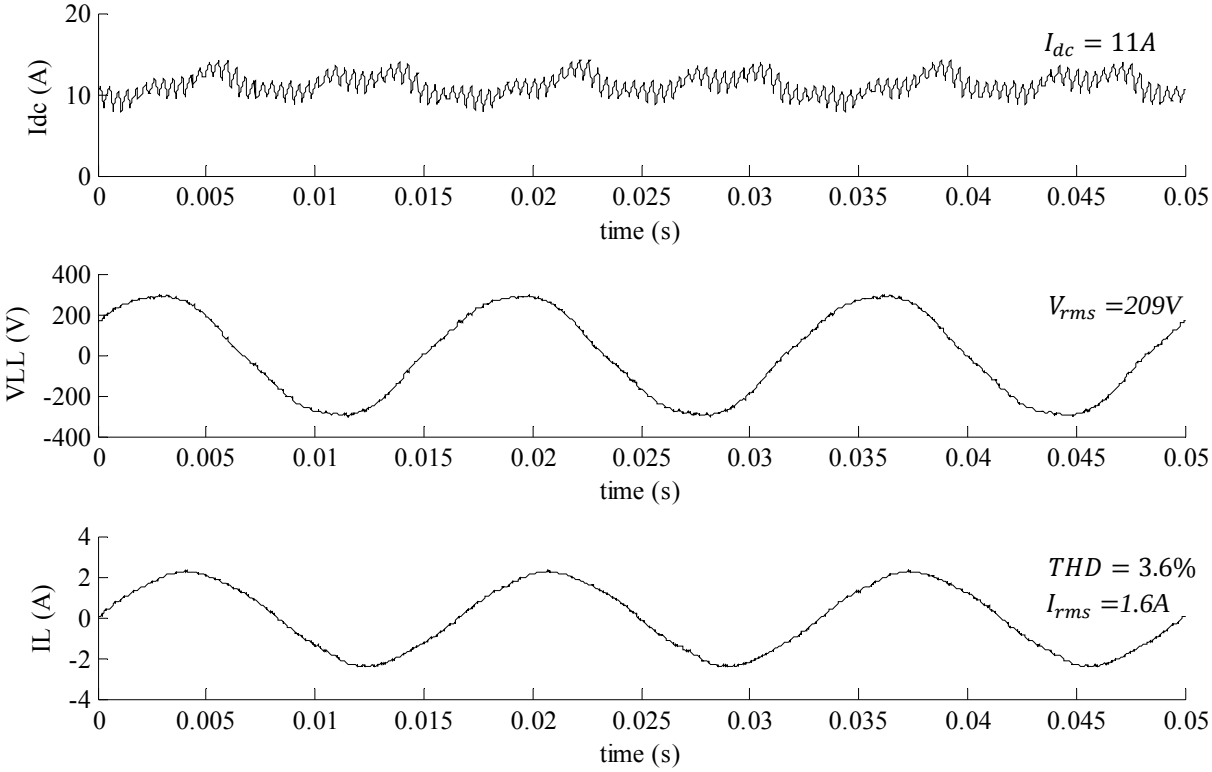


Figure 7-14 Experimental Results for V_{dc}=70V, C_{ac}=20µF and R_{load}=75Ω

7.3.7 Experimental Results for V_{dc}=75V

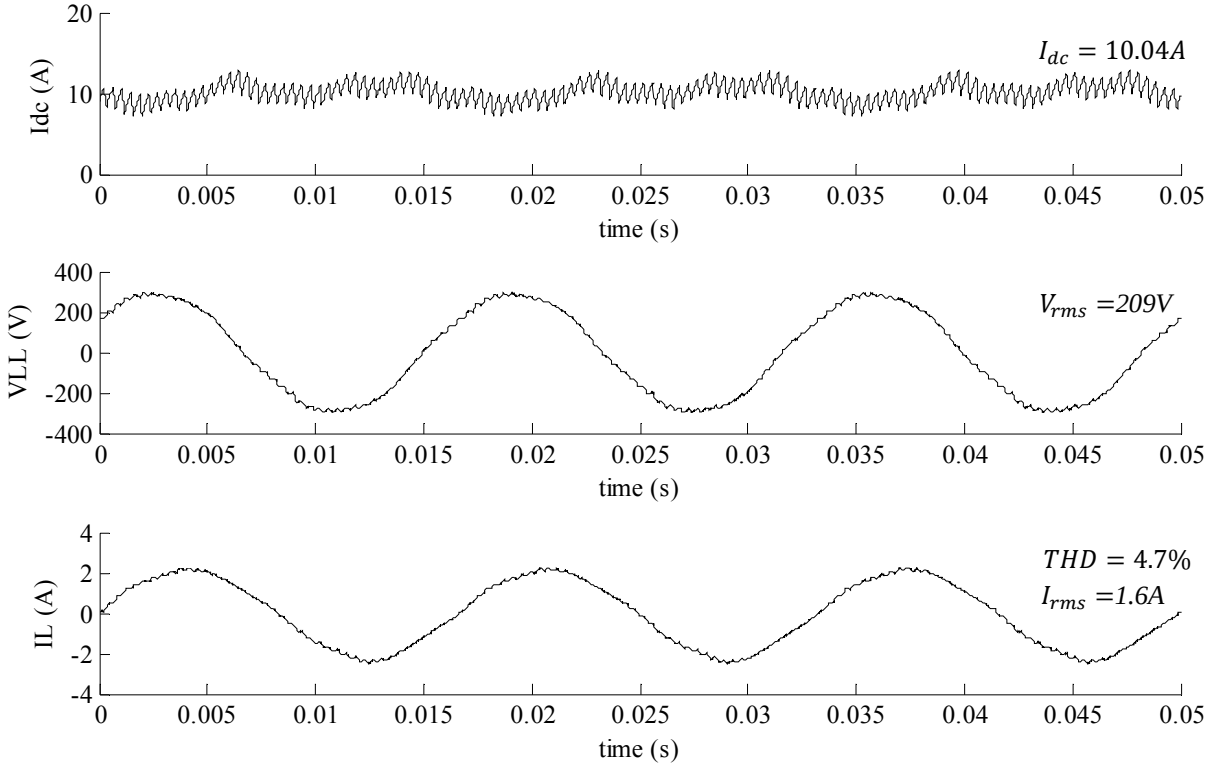


Figure 7-15 Experimental Results for V_{dc}=75V, C_{ac}=10µF and R_{load}=75Ω

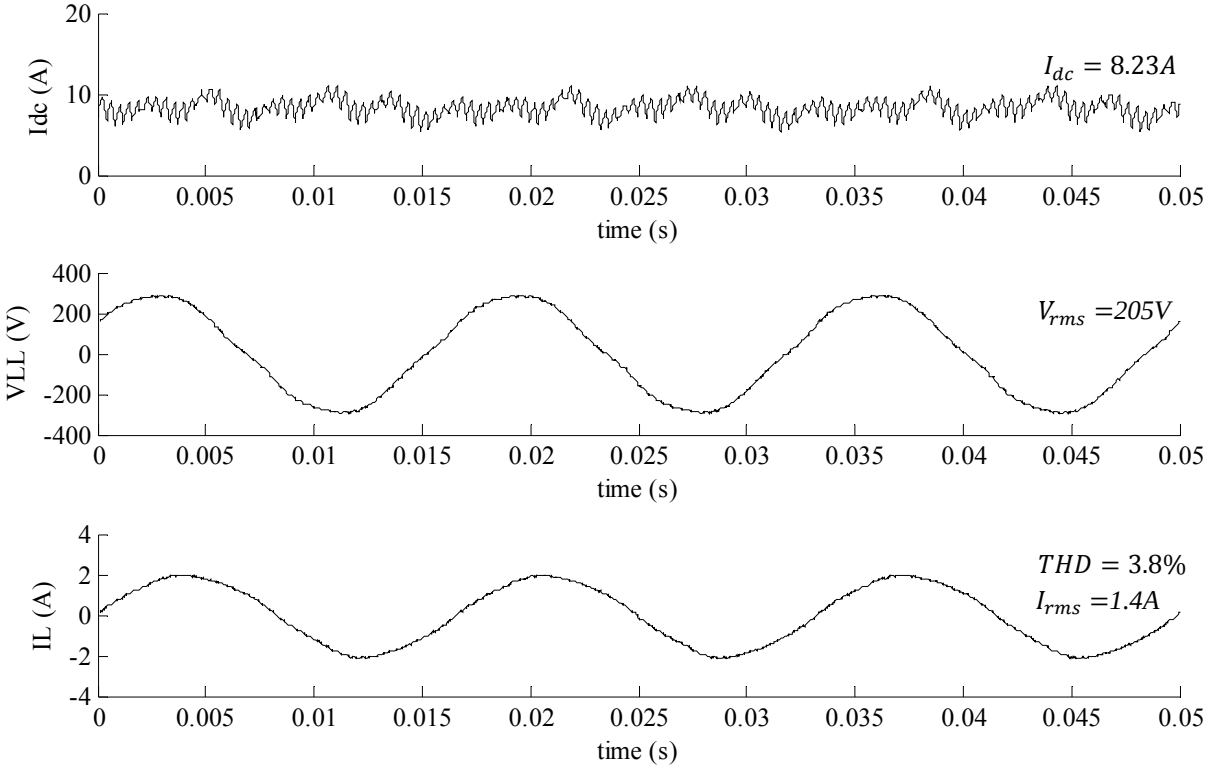


Figure 7-16 Experimental Results for V_{dc}=75V, C_{ac}=20µF and R_{load}=85Ω

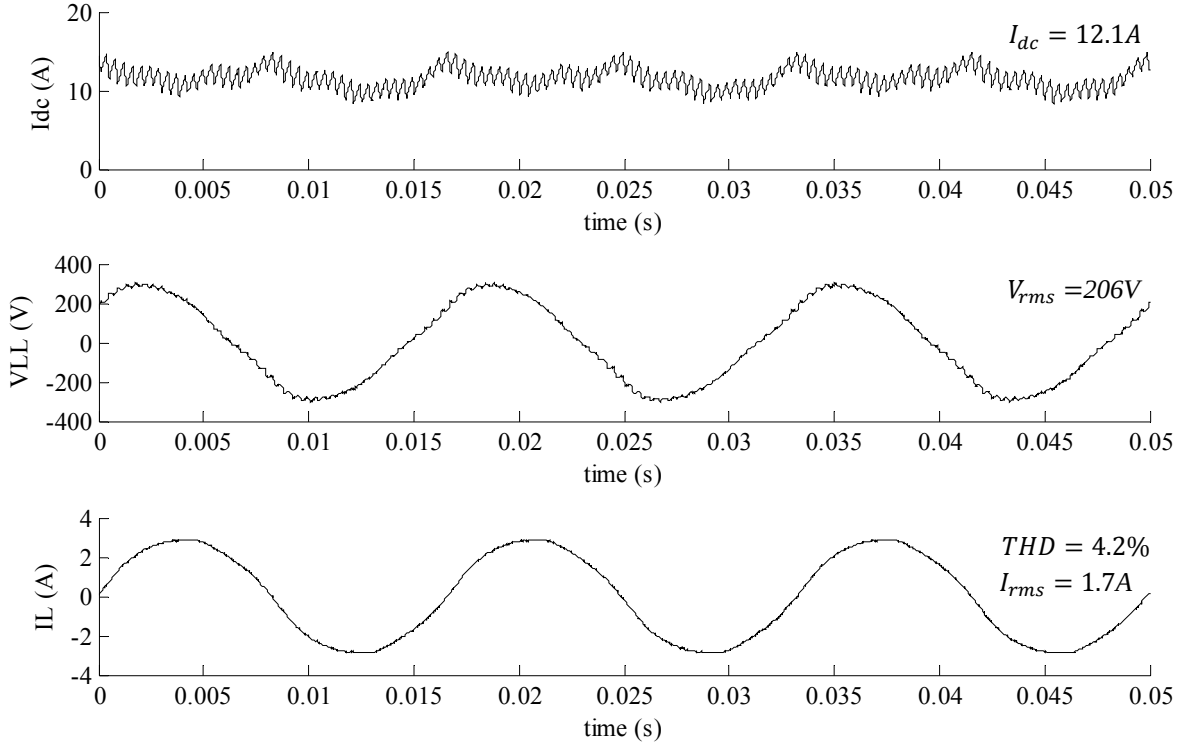


Figure 7-17 Experimental Results for V_{dc}=75V, C_{ac}=20µF, R_L=50Ω & L_L=17.5mH

7.3.8 Experimental Results for V_{dc}=80V

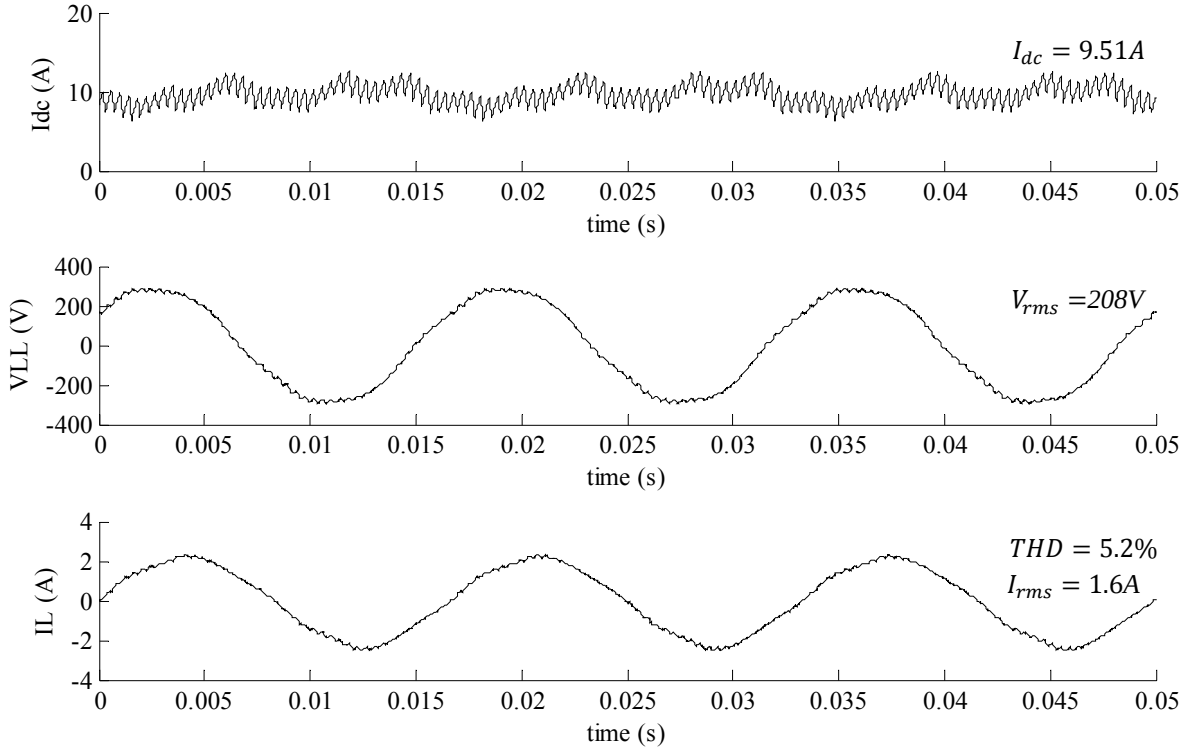


Figure 7-18 Experimental Results for V_{dc}=80V, C_{ac}=10µF and R_{load}=75Ω

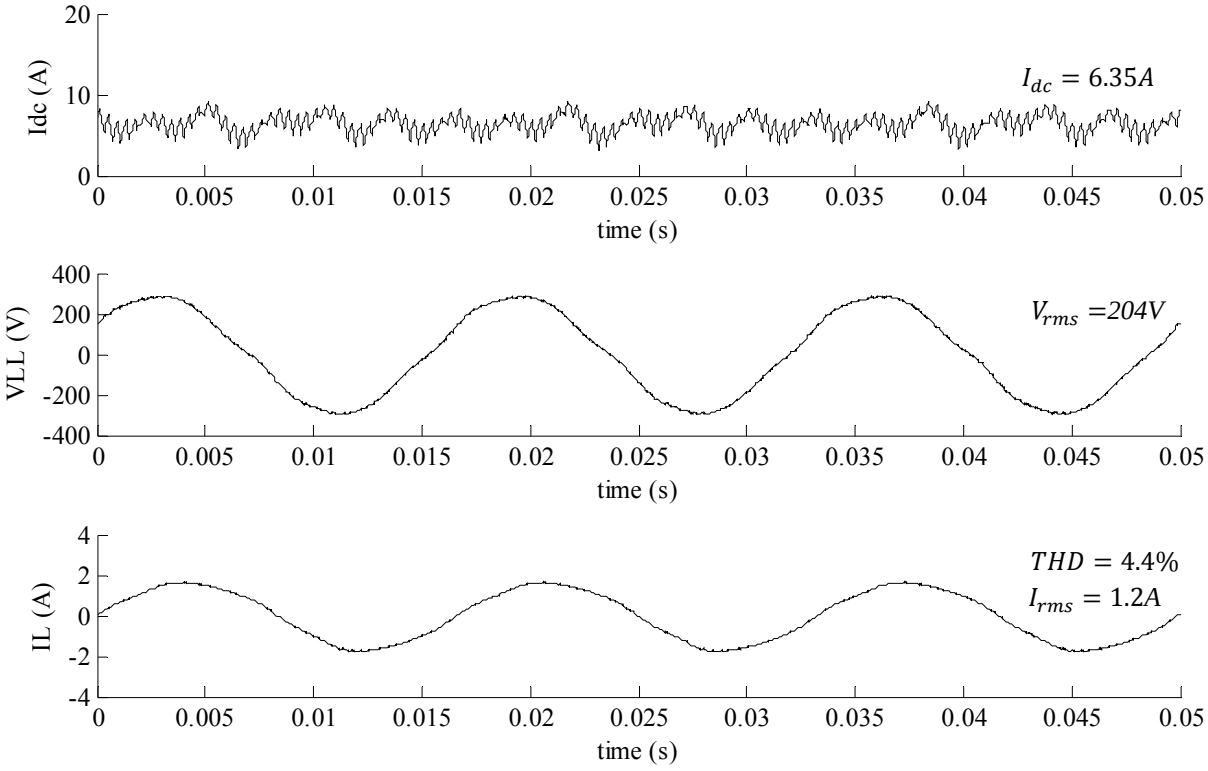


Figure 7-19 Experimental Results for V_{dc}=80V, C_{ac}=20μF and R_{load}=100Ω

7.3.9 Experimental Results for an Inductive Load

In this case, an induction machine was connected as the load of the inverter. The inverter was working with V_{dc}=65V and C_{ac}=10μF. Table 7-3 provides the specifications of this machine which was running in no load condition. Figure 7-20 gives line to line voltage across the machine. The first plot shows line to line voltage when it is connected to the inverter and second plot gives the line to line voltage when it is connected to the grid.

Table 7-3 Specifications of the Induction Machine

Make	MagneTek (Century AC Motor) HM2H003
Rated Voltage	200-230/460V
Rated Current	1.4-1.6/0.8
RPM	1725/1425
frequency	60/50Hz

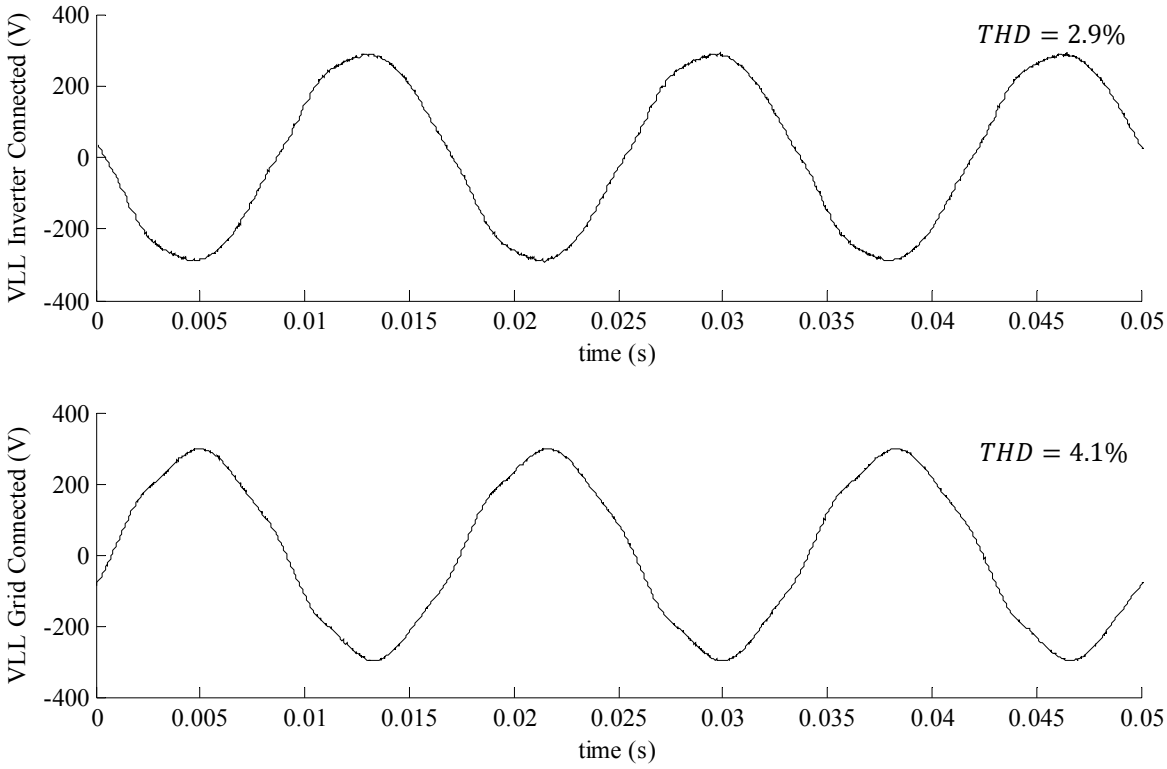


Figure 7-20 Line to Line Voltage of the Induction Machine connected to a) Inverter b) Electric Grid

7.4 Discussion of Experimental Results

As shown in Figure 7-5 through Figure 7-19, experimental results verify the switching pattern and simulation results derived in the previous chapter. In all cases, the rms value of the line to line output voltage is within 3% of the desired rms value (208v), demonstrating that the output voltage perfectly follows the reference signal. Also, THD of the output current is less than the expected level, 5% [24].

A table including all simulated and experimental results for several other experiments has been provided in Appendix D. Figure 7-21 shows the relation between the load and charging ratio. This figure shows the curves for only three loads to prevent too many lines in the figure. As expected and demonstrated in Figure 7-21, as the load increases, the charging ratio decreases to maintain the output voltage at a desired level. The reason that, in some cases, the charging ratio is the same for two different loads in the same input voltage is that because of the system resolution, the number of charging points needed to keep the output voltage at a desired level (closest to the required value) is equal. Although the number of charging points is equal, the

rms value of the output voltage is higher for a higher load. For example, rms of line to line voltage is 202V when V_{dc}=55V and Load=80Ω, while it is 210V when V_{dc}=55V and Load=90Ω although in both cases, the charging ratio is 0.71.

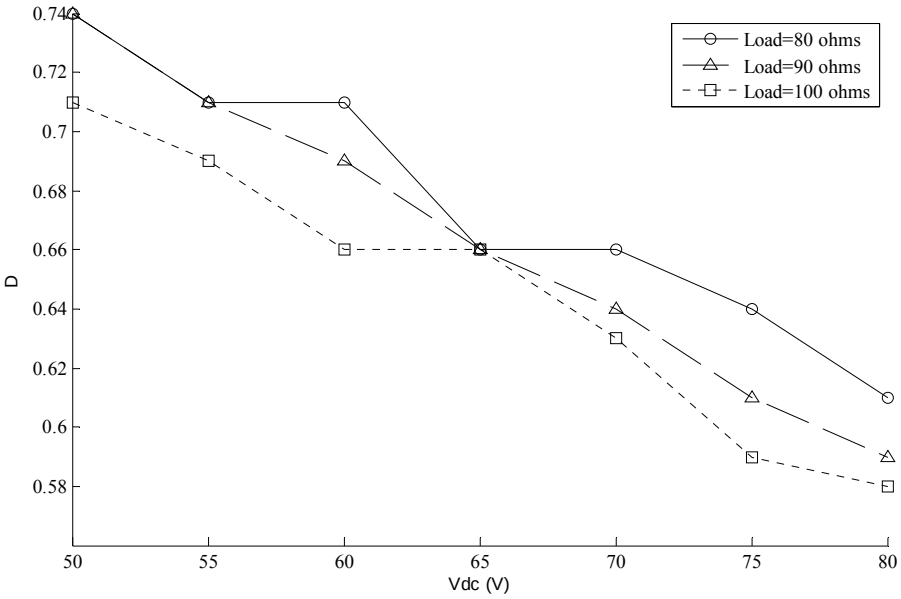


Figure 7-21 Relationship between Input DC Voltage and Charging Ratio (C_{ac}=10μF)

7.5 Conclusion

In this chapter, experimental results of applying modified phasor pulse width modulation for a 1kW, 208V_{LL} three-phase boost inverter were presented. The experimental results are in good agreement with the switching pattern developed in Chapter 5 and simulation results presented in Chapter 6.

Chapter 8 - Conclusion and Future Work

In this chapter, a summary of the accomplishments of this work and main contributions of this thesis are given. At the end of the chapter, some suggestions for future work are given.

8.1 Summary and Accomplishments

Several interface options for connecting PV systems to electric grid or local load are available such as voltage source inverter (VSI), interface circuit using a transformer, interface circuit using a DC-DC converter in series with a VSI, multilevel inverter, impedance-source (z-source) inverter and boost inverter. All of these interface circuits have their own advantages and disadvantages. However, the ability of the three-phase single-stage boost inverter in boosting and inverting input DC voltage into a sinusoidal AC voltage in one stage reduces the number of solid-state switches and eliminates the use of electrolytic capacitors, which enhance the reliability of PV systems. This was the main motivation in investigating this type of interface circuit in this work.

After an introductory chapter, Chapter 1, in which motivation of this work, a brief literature review and problem statement were presented, in Chapter 2 and Chapter 3, overview of some basic materials needed in this work were given. In Chapter 2, a brief discussion on different types of interface circuits for photovoltaic systems and their advantages and disadvantages was presented. In Chapter 3, fundamentals of major pulse width modulation (PWM) techniques were reviewed. In Chapter 4 of this thesis, the integration of DC link inductor of boost inverter with a PV panel was achieved for single-stage boost inverters. In this work, ANSYS Q3D software was applied to integrate an inductor with an inductance value of approximately 68mH into 'Astronergy CHSM6610M' PV panel. The integrated inductor was modeled as an air-core coil on the back of each PV cell. Several configurations of wiring were investigated using ANSYS Q3D software and the result of one of the simulations showed that an inductor with an inductance value of approximately 1.14mH can be built on the back of each PV cell. While the PV panel used in this work has 60 cells, therefore, by connecting these inductors in series, an inductance value of around 68mH was achieved which exceeds the required value of the DC link inductor of a 1kW single-stage boost inverter. In Chapter 5, phasor pulse width modulation (PPWM) switching method was reviewed. This method is based on the concept of space vector PWM (SVPWM), but the switching pattern is generated based on the inverter output line to line voltage phasors. The problem associated with this

method rises when a low-resolution processor is used to generate the switching pattern. Low resolution processor causes some pulse dropping in the generated switching pattern which results in some asymmetric conditions in the output voltage and current waveforms of the inverter, and consequently an increase in THD of these waveforms. In order to solve this problem, a modified PPWM method was developed in this thesis which guarantees the symmetric condition in the switching pattern by discretizing the discharging time intervals in every switching cycle.

In order to verify this new proposed method, the boost inverter along with the proposed switching pattern was implemented using Matlab/Simulink software. Moreover, the proposed switching pattern was implemented using a $1kW, 208V_{LL_{rms}}$ laboratory-scale three-phase boost inverter. The simulated and experimental results presented in Chapter 6 and Chapter 7, respectively, confirm the effectiveness of the proposed PWM technique for single-stage boost inverters. These results demonstrated that the proposed switching pattern can be applied in a wide range of input DC voltages and different loads. Moreover, a comparison between the results of PPWM and modified PPWM methods showed a significant improvement in THD of output line to line voltage and line current waveforms.

8.2 Future Work

In the future, this modified version of phasor pulse width modulation can also be applied to the boost inverter for grid-tied applications. In this case, photovoltaic panels can be used to provide power to the grid. Also, the effectiveness of the inverter can be increased by using a FPGA-based system for generating the switching pattern. FPGA-based systems can work with much higher frequency than dSPACE, therefore, the system can be tested with smaller step size, thus increasing the resolution of the system and decreasing the losses and total harmonic distortion (THD) of output voltage and current waveforms.

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Appendix A - PCB Design Information

In this appendix, a printout of the printed circuit board prototypes that were designed for the boost inverter is presented.

The designed boost inverter consists of two boards:

1) Signal board
2) Power board

Separating the signal board from the power has notably decreased the amount of electromagnetic interference (EMI) in the system.

Figure A-1 shows an image of the designed signal board.

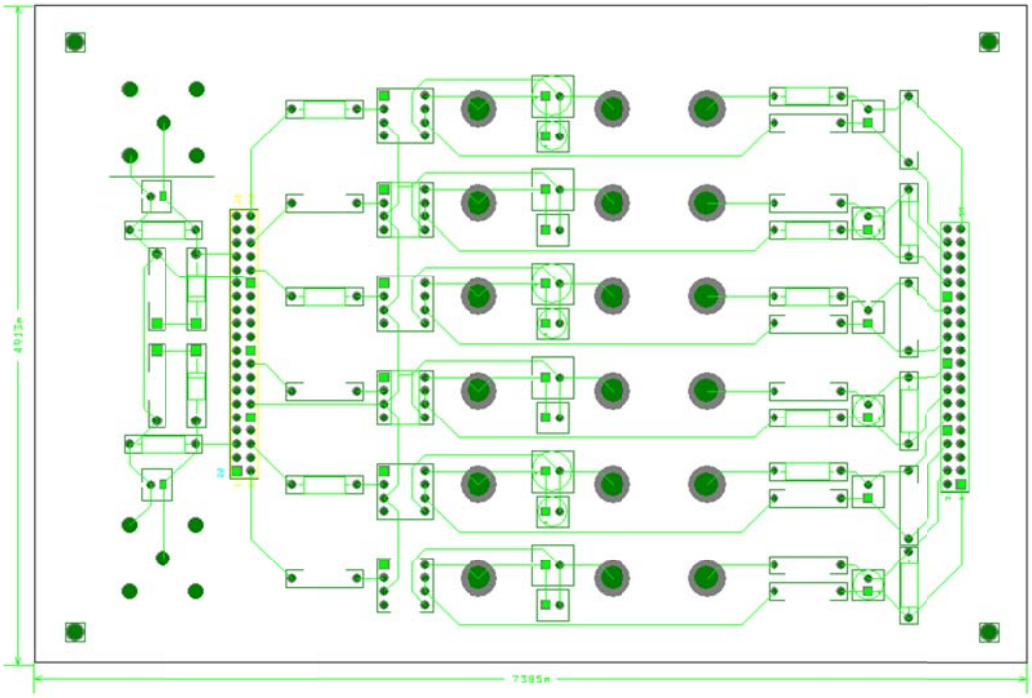

Figure A-1 Signal Board PCB Layout

In this picture, the BNC, resistor, and Zener diode footprints are used to feedback signals from the circuit. A 40-pin footprint has been used as the input of the circuit. This footprint is used to connect the output of the FPGA to the signal board. This 40-pin footprint was used to connect to six gate drive circuits which produce gating signals for switches used in the power board of the inverter.

The power board is shown in Figure A-2.

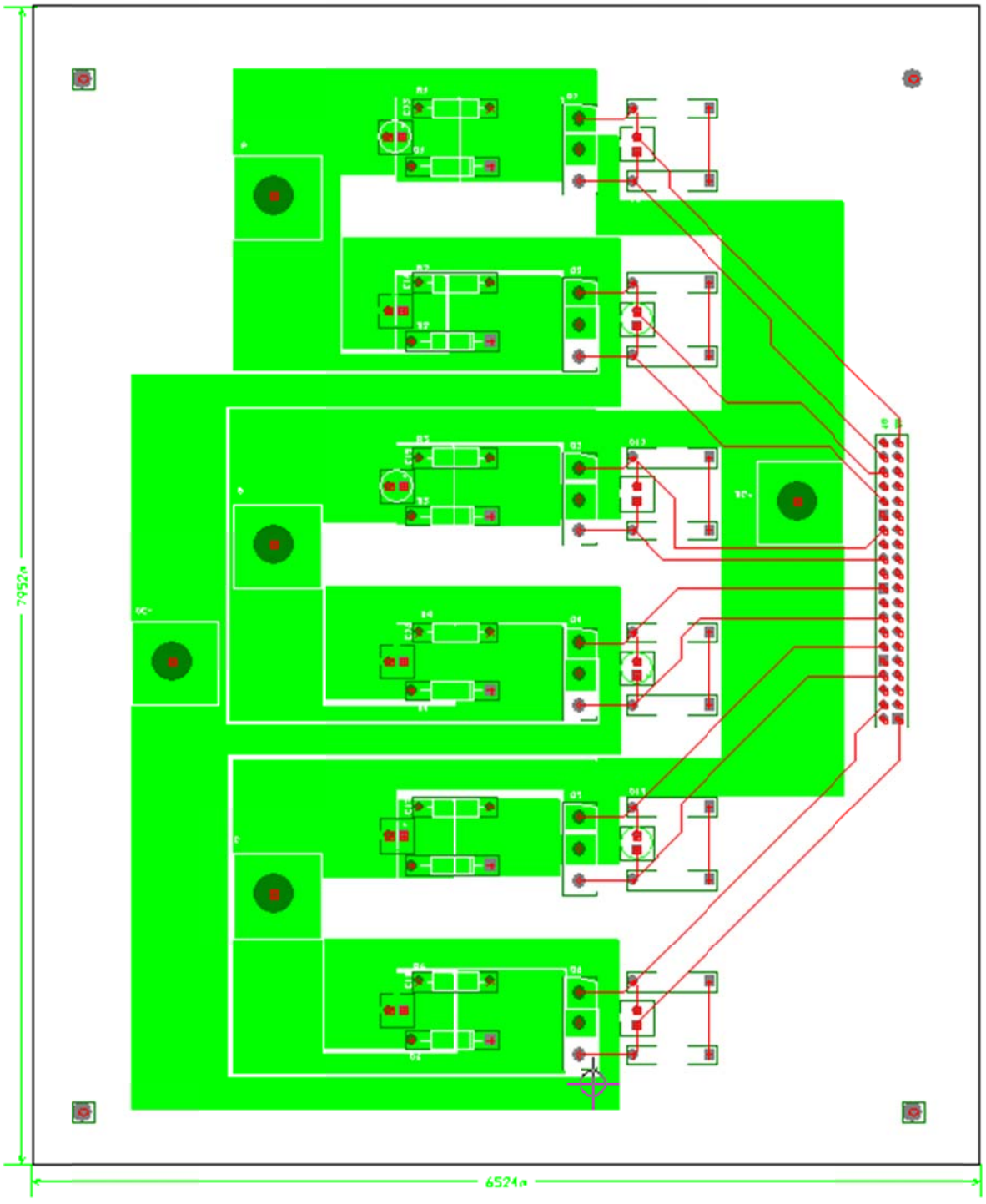

Figure A-2 Power Board PCB Layout

The output of the signal board, which is the 40-pin footprint in Figure A-1 is the input of the power board. Signals are connected to gate and emitter of the switches in the power board.

Red lines in Figure A-2 present the signals, while green areas in this figure show the copper areas used for power circuit.

After designing the PCB layouts, the final step is a review of the design. This process is called DFM check (Design for Manufacturability check). This process checks the layouts for any violations of spacing, misconnection, etc.

If the DFM check shows no violations in the design, the design can be sent to any of the PCB manufacturing companies.

Appendix B - Simulink Model

In this appendix, various parts of the Simulink model used for simulation and experimental results are presented.

Figure B-1 shows the Simulink model used.

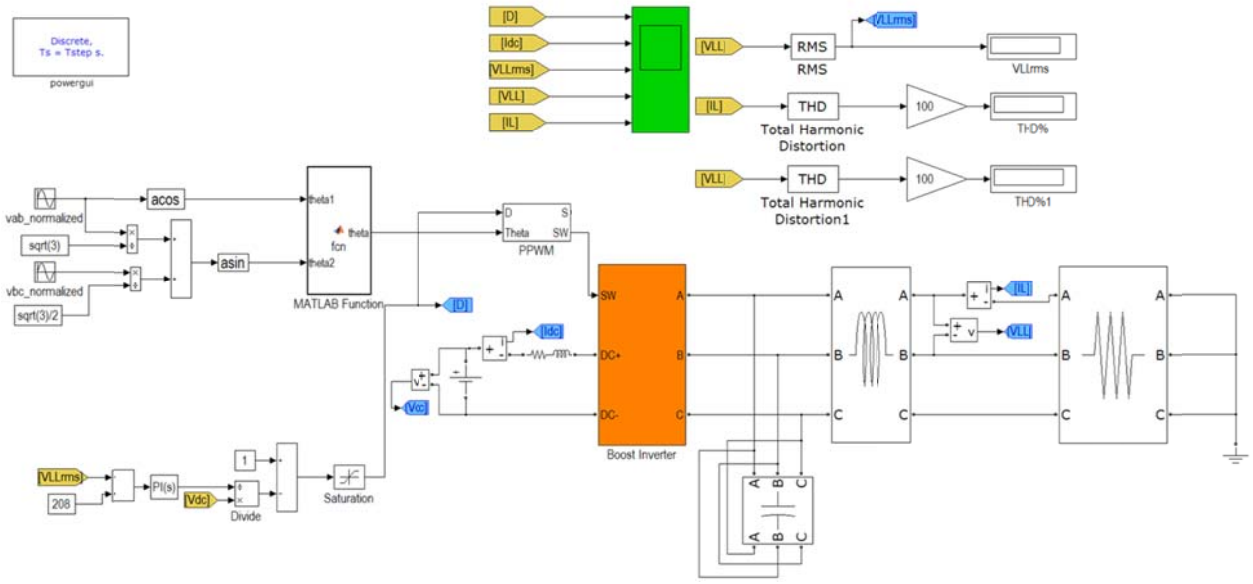

Figure B-1 Simulink Model Used for Simulation and Experimental Purposes

The Simulink model has been discussed in detail in Chapter 5. In this appendix, the MATLAB codes used in this model are presented.

The MATLAB code in 'MATLAB Function' block which produces the phasor of the output voltage is as follows:

```
function theta =fcn(theta1,theta2)
theta=0;
 if theta1<=pi/2
     if theta2>=0
         theta=theta1;
     else
         theta=2*pi+theta2;
     end
 elseif theta1>pi/2
     if theta2>=0
         theta=theta1;
     else
         theta=pi-theta2;
     end
 end
```

Blocks in PPWM block are shown in Figure B-2 below.

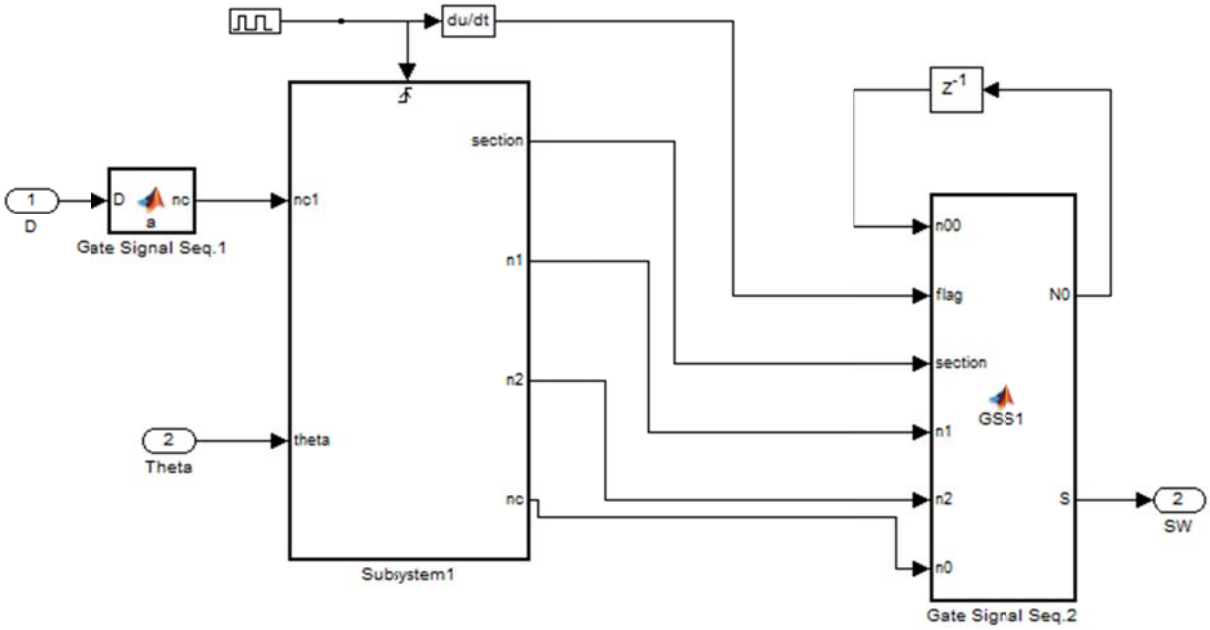

Figure B-2 Simulink Blocks Inside PPWM Block

The 'Subsystem1' block inputs are 'theta' (phasor of the output signal) and 'n_c' (charging points), and its outputs are 'section' (sector that the system is working in), 'n_c' (modified charging points), 'n_1' (discharging points in first interval), 'n_2' (discharging points in second interval). The MATLAB code in this block is as follows:

```
function [sec,n1,n2,nc] = fcn(theta,nc1)
ntotal=41;
n1=0;
n2=0;
nc=0;
if theta<=pi/3
    sec=1;
    theta1=theta;
elseif theta<=2*pi/3
    sec=2;
    theta1=theta-pi/3;
elseif theta<=pi
    sec=3;
    theta1=theta-2*pi/3;
elseif theta<=4*pi/3
    sec=4;
    theta1=theta-pi;
elseif theta<=5*pi/3
    sec=5;
    theta1=theta-4*pi/3;
else
    sec=6;
    theta1=theta-5*pi/3;
```

```
end
if theta1<=6*pi/180
        n1=ntotal-nc1;
        n2=0;
        nc=nc1;
elseif theta1<=12*pi/180
        n1=floor(8*(ntotal-nc1)/9);
        n2=floor(1*(ntotal-nc1)/9);
        nc=nc1+(ntotal-(nc1+n1+n2));
elseif theta1<=18*pi/180
        n1=floor(7*(ntotal-nc1)/9);
        n2=floor(2*(ntotal-nc1)/9);
        nc=nc1+(ntotal-(nc1+n1+n2));
elseif theta1<=24*pi/180
        n1=floor(6*(ntotal-nc1)/9);
        n2=floor(3*(ntotal-nc1)/9);
        nc=nc1+(ntotal-(nc1+n1+n2));
elseif theta1<=30*pi/180
        n1=floor(5*(ntotal-nc1)/9);
        n2=floor(4*(ntotal-nc1)/9);
        nc=nc1+(ntotal-(nc1+n1+n2));
elseif theta1<=36*pi/180
        n1=floor(4*(ntotal-nc1)/9);
        n2=floor(5*(ntotal-nc1)/9);
        nc=nc1+(ntotal-(nc1+n1+n2));
elseif theta1<=42*pi/180
        n1=floor(3*(ntotal-nc1)/9);
        n2=floor(6*(ntotal-nc1)/9);
        nc=nc1+(ntotal-(nc1+n1+n2));
elseif theta1<=48*pi/180
        n1=floor(2*(ntotal-nc1)/9);
        n2=floor(7*(ntotal-nc1)/9);
        nc=nc1+(ntotal-(nc1+n1+n2));
elseif theta1<=54*pi/180
        n1=floor(1*(ntotal-nc1)/9);
        n2=floor(8*(ntotal-nc1)/9);
        nc=nc1+(ntotal-(nc1+n1+n2));
else
        n1=0;
        n2=ntotal-nc1;
        nc=nc1;
end
```

Also, the ‘Gate Signal Seq2’ block inputs are the outputs of ‘Subsystem1’ block, ‘flag’ (shows the beginning of a switching cycle), and ‘n_{00}’ (internal counter of block). The output of the block is the switching pattern for switches used in the inverter. The MATLAB code used in this block is as follows:

```
function [N0,S] = GSS1(n00,flag,section,n1,n2,n0)
S=[0;0;0;0;0;0];
if flag < -10
    n=0;
else
    n=n00;
```

```
end
if  section ==1
    if n<n0
        S=[1;1;0;0;0;0];
    elseif n==n0
        S=[1;1;0;1;0;0];
    elseif n<(n0+n1) && n>n0
        S=[1;0;0;1;0;0];
    elseif n==n0+n1
        S=[1;0;0;1;0;1];
    else
        S=[1;0;0;0;0;1];
    end
end
if  section ==2
    if n<n0
        S=[0;0;0;0;1;1];
    elseif n==n0
        S=[1;0;0;0;1;1];
    elseif n<(n0+n1) && n>n0
        S=[1;0;0;0;0;1];
    elseif n==n0+n1
        S=[1;0;1;0;0;1];
    else
        S=[0;0;1;0;0;1];
    end
end
if  section ==3
    if n<n0
        S=[0;0;1;1;0;0];
    elseif n==n0
        S=[0;0;1;1;0;1];
    elseif n<(n0+n1) && n>n0
        S=[0;0;1;0;0;1];
    elseif n==n0+n1
        S=[0;1;1;0;0;1];
    else
        S=[0;1;1;0;0;0];
    end
end
if  section ==4
    if n<n0
        S=[1;1;0;0;0;0];
    elseif n==n0
        S=[1;1;1;0;0;0];
    elseif n<(n0+n1) && n>n0
        S=[0;1;1;0;0;0];
    elseif n==n0+n1
        S=[0;1;1;0;1;0];
    else
        S=[0;1;0;0;1;0];
    end
end
if  section ==5
    if n<n0
        S=[0;0;0;0;1;1];
    elseif n==n0
```

```
        S=[0;1;0;0;1;1];
    elseif n<(n0+n1) && n>n0
        S=[0;1;0;0;1;0];
    elseif n==n0+n1
        S=[0;1;0;1;1;0];
    else
        S=[0;0;0;1;1;0];
    end
end
if  section ==6
    if n<n0
        S=[0;0;1;1;0;0];
    elseif n==n0+n1
        S=[0;0;1;1;1;0];
    elseif n<(n0+n1) && n>n0
        S=[0;0;0;1;1;0];
    elseif n==n0+n1
        S=[1;0;0;1;1;0];
    else
        S=[1;0;0;1;0;0];
    end
end
n=n+1;
N0=n;
```

The ‘Boost Inverter’ block has six switches that are in series with diodes. Figure B-3 shows elements used inside this block.

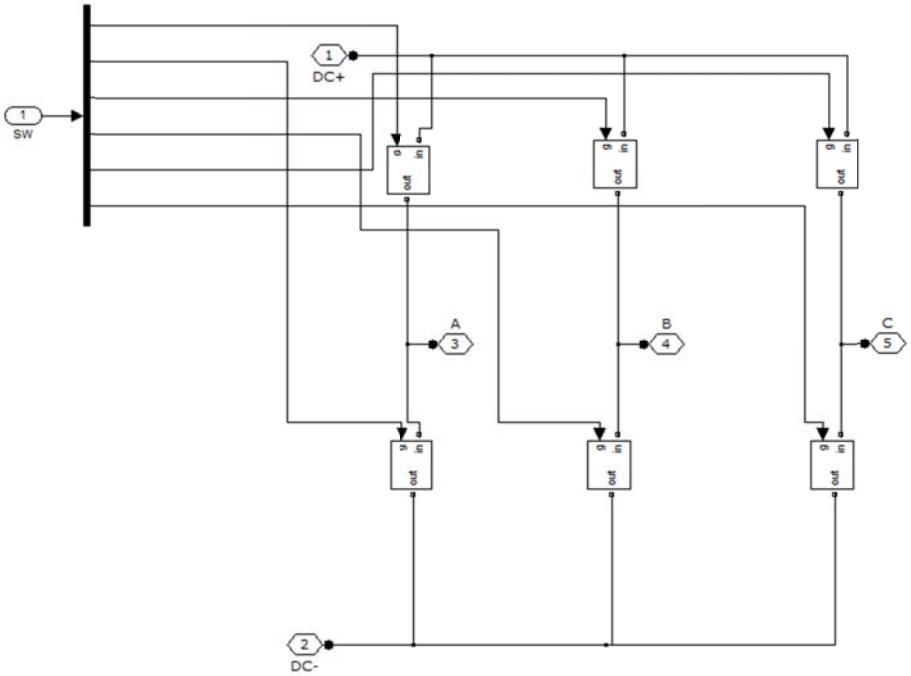

Figure B-3 Simulink Blocks Representing the inverter

The blocks inside each switch model are shown in Figure B-4. As it can be seen, each block consists of a switch in series with a diode.

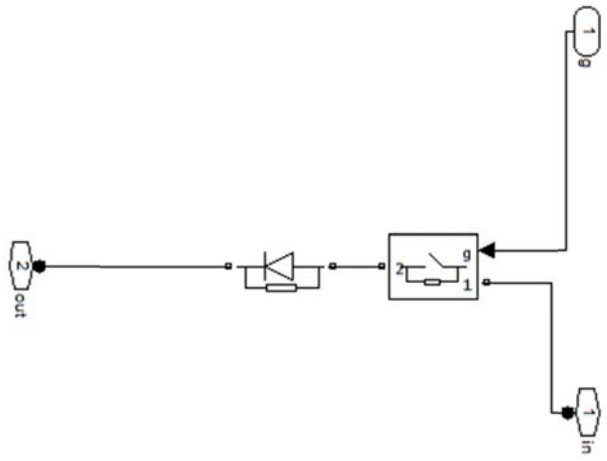

Figure B-4 IGBT and Diode Model in the Inverter

Appendix C - Gate Drive and Snubber Circuit

Gate Drive Circuit

The circuit shown in Figure C-1 was used for gate drive circuits for inverter switches. Values of the components in the circuit are given in Table C-1. The output signal of this circuit has two levels. It produces a positive voltage level to turn the switch ON and a negative voltage level to turn the switch OFF.

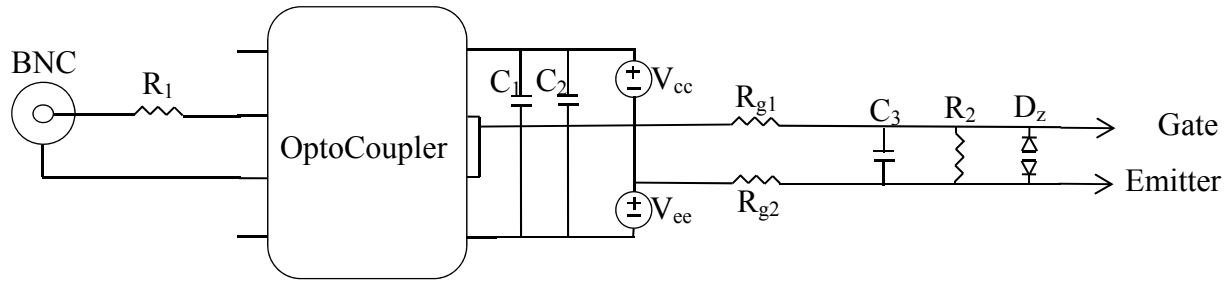

Figure C-1 Gate Drive Circuit Used in the Inverter

Table C-1 Gate Drive Circuit Component Values

R1	270Ω
R2	10kΩ
R_{g1}	5.6Ω
R_{g2}	5.6Ω
C_1	0.1μF
C_2	47μF
C_3	100nF
D_z	18v Zener Diodes
OptoCoupler	Fairchild 3120 (1039B)
V_{cc}, V_{ee}	18v, 7v

Based on the datasheet of the Optocoupler, R_{g1} and R_{g2} should be chosen such that:

$$R_{g1}, R_{g2} > \frac{V_{cc} - V_{ee} - V_{OL}}{2 * I_{OL,Peak}} = \frac{18 - (-7) - 2}{2 * 2.5} = 4.6\Omega \qquad (C.1)$$

In the equation above, V_{OL} and I_{OL} are the Optocoupler output voltage and current, respectively. The V_{OL} value of 2v is a conservative value of V_{OL} at the peak current of 2.5A. Figure C-2 shows the performance of the gate drive circuit. In this figure, the top signal shows the output of

dSPACE while the bottom signal is the output of gate drive circuit (the signal that should be applied to the gate and emitter of the switch).

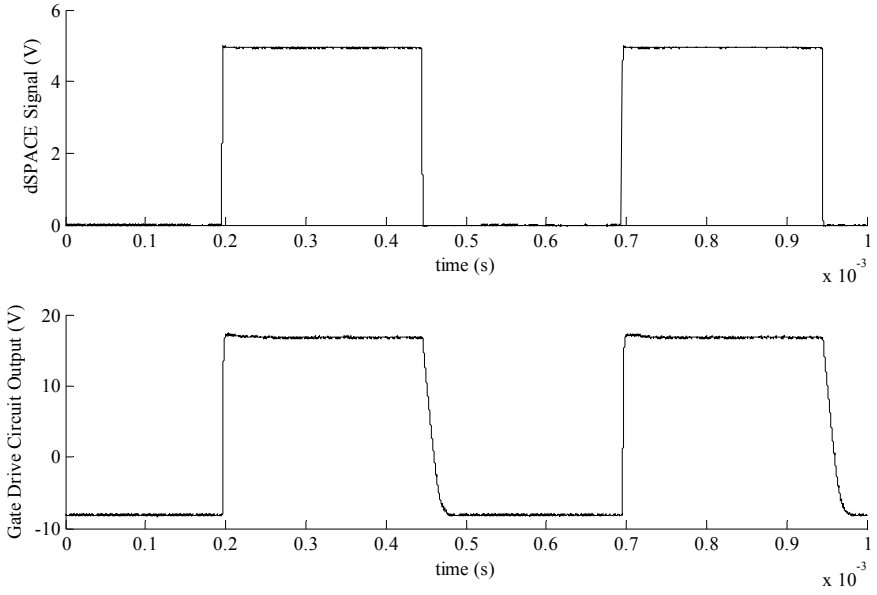

Figure C-2 Gate Drive Circuit Output Signal

While the switches that have been used in the inverter turn on at a V_{ge} of 2.5-6v, two time durations are important to note:

1) The time period between when dSPACE signal becomes low (turn OFF signal) and when V_{ge} becomes 2.5 volts (switch is definitely OFF): This time is approximately 11μs.
2) The time period between when dSPACE signal becomes high (turn ON signal) and when V_{ge} becomes 6 volts (switch is definitely ON): This time is approximately 1.6μs.

Snubber Circuit

A turn-off snubber circuit has been used to make the voltage across the switch zero when it turns off. The configuration of a turn-off snubber circuit is shown in Figure C-3.

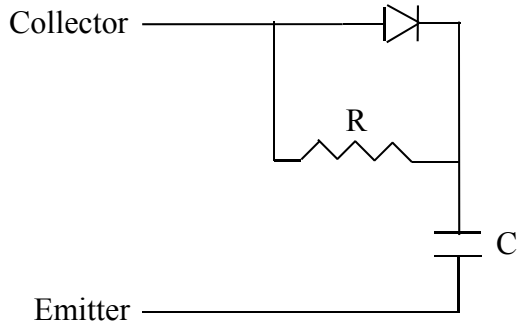

Figure C-3 Snubber Circuit Used in the Inverter

The value of circuit components in the snubber circuit is given in Table C-2.

Table C-2 Snubber Circuit Component Values

R	30Ω
C	33nF
Diode	1N4007

Performance of the snubber circuit has been studied by applying a DC voltage across the switch in series with a resistor. Results have been given in Figure 7-10. The first row shows the dSPACE input signal, while the second row shows voltage across the collector and emitter of the switch. As can be seen, when the switch turns off, there is no spike in the voltage between collector and emitter and it smoothly goes up until it reaches its final value.

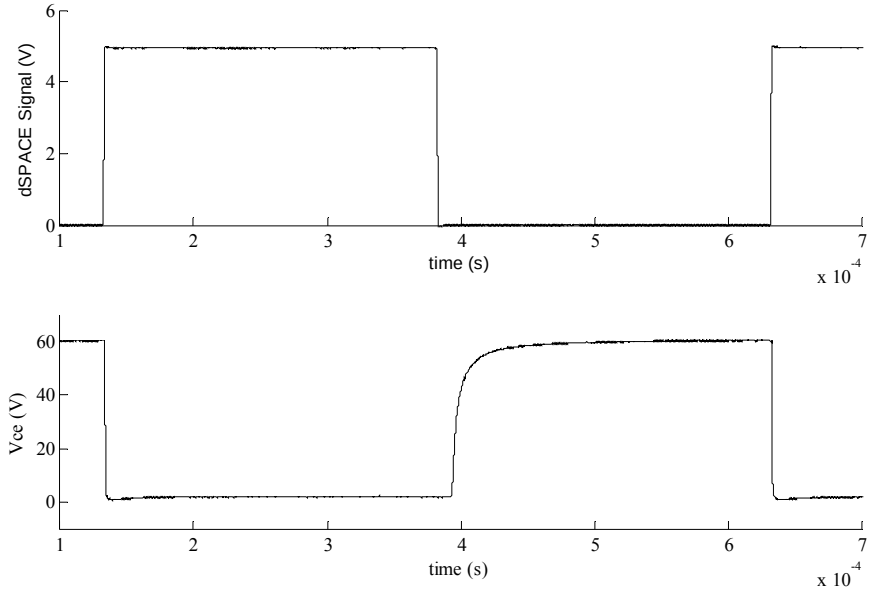

Figure C-4 Snubber Circuit Performance Evaluation

Appendix D - Simulation and Experimental Data

				Simulation Results					Experimental Results							
V_{dc} (V)	C_{ac} (μF)	Load (Ω)	L_{filter} (mH)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	P_{in} (W)	P_{out} (W)	Eff (%)
50	10	75	7.5	0.74	13	4.34	213	1.69	0.75	13.95	5.1	201	1.6	697.5	531.5	76.2
50	10	80	7.5	0.74	13	4.38	219	1.66	0.74	13.7	4.9	204	1.4	685	526.4	76.8
50	10	85	7.5	0.73	10	4.46	197	1.41	0.74	13.6	4.6	207.7	1.3	680	517.5	76.1
50	10	90	7.5	0.73	10	4.44	202	1.37	0.74	13.44	4.7	209	1.3	672	514	76.5
50	10	95	7.5	0.73	10	4.35	208	1.34	0.74	13.47	4.7	215	1.2	673.5	510.4	75.8
50	10	100	7.5	0.7	9	4.32	203	1.2	0.71	10.7	4.2	202	1.2	535	411.8	77
50	20	75	7.5	0.61	12	3.46	208	1.66	0.66	15.05	3.2	208	1.5	752.5	585	77.7
50	20	80	7.5	0.6	11	3.64	206	1.62	0.66	15.17	3.3	213	1.5	758.5	587.8	77.5
50	20	85	7.5	0.59	11	3.61	216	1.41	0.64	13.23	3.1	209	1.4	661.5	515.9	78

				Simulation Results						Experimental Results						
V_{dc} (V)	C_{ac} (μF)	Load (Ω)	L_{filter} (mH)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	P_{in} (W)	P_{out} (W)	Eff (%)
50	20	90	7.5	0.58	10	3.06	208	1.34	0.64	13.42	3.1	216	1.3	671	521.3	77.7
50	20	95	7.5	0.54	10	3.25	213	1.31	0.61	12.24	3	205	1.3	612	476.4	77.8
50	20	100	7.5	0.52	9	3.57	212	1.24	0.61	12.56	3.5	212	1.2	628	485.2	77.3
55	10	75	7.5	0.73	11	4.53	204	1.7	0.74	15.13	5.1	216	1.5	832.1	641.6	77.1
55	10	80	7.5	0.71	11	4.4	210	1.56	0.71	12.08	4.7	202	1.4	664.4	517.9	77.9
55	10	85	7.5	0.7	9.5	4.4	205	1.45	0.71	12	4.2	208	1.4	660	513.7	77.8
55	10	90	7.5	0.7	9	4.5	211	1.41	0.71	11.9	4.7	212	1.3	654.5	511.1	78.1
55	10	95	7.5	0.68	8	4.31	203	1.27	0.71	11.73	4.7	208	1.3	654.1	500.6	77.6
55	10	100	7.5	0.68	8	4.3	209	1.27	0.69	10.1	4.6	199	1.1	555.6	436	78.5

				Simulation Results						Experimental Results						
V_{dc} (V)	C_{ac} (μF)	Load (Ω)	L_{filter} (mH)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	P_{in} (W)	P_{out} (W)	Eff (%)
55	20	75	7.5	0.59	11.5	3.59	215	1.7	0.64	13.76	3	206	1.5	756.8	600.3	79.3
55	20	80	7.5	0.58	10	3.02	208	1.52	0.61	12.57	3.2	202	1.3	691.3	550.4	79.6
55	20	85	7.5	0.53	9	3.5	204	1.41	0.61	12.9	3.1	211	1.4	709.5	563.6	79.4
55	20	90	7.5	0.52	9	3.53	213	1.38	0.59	11.64	3.1	207.1	1.3	640.2	509	79.5
55	20	95	7.5	0.5	8.5	3.57	209	1.27	0.59	11.88	3.3	212	1.3	653.4	518.1	79.3
55	20	100	7.5	0.48	8	3.95	209	1.27	0.57	10	2.7	201	1.2	550	436	79.3
60	10	75	7.5	0.69	10	4.48	210	1.7	0.71	13.13	4.8	205	1.5	787.8	613.9	77.9
60	10	80	7.5	0.68	9	4.41	202.5	1.56	0.71	12.94	4.5	210	1.5	776.4	604.5	77.8
60	10	85	7.5	0.68	9	4.37	209	1.41	0.69	11.05	5.1	203	1.3	663	524.4	79.1

				Simulation Results						Experimental Results						
V_{dc} (V)	C_{ac} (μF)	Load (Ω)	L_{filter} (mH)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	P_{in} (W)	P_{out} (W)	Eff (%)
60	10	90	7.5	0.66	9	4.34	215	1.48	0.69	11	4.9	208	1.3	660	520.6	78.9
60	10	95	7.5	0.65	7	4.34	203	1.31	0.69	10.98	4.8	212	1.3	658.8	516.5	78.4
60	10	100	7.5	0.65	7.5	4.32	209	1.27	0.66	9.4	4.3	203	1.2	564	445.9	79.1
60	20	75	7.5	0.54	10	3.18	212	1.66	0.61	13.46	3.4	214	1.6	807.6	645.4	79.9
60	20	80	7.5	0.53	9	3.49	212	1.56	0.59	12.04	3.4	208	1.5	722.4	580.9	80.4
60	20	85	7.5	0.51	8.5	3.55	208	1.45	0.59	12.33	3.6	213	1.4	739.8	588.3	79.5
60	20	90	7.5	0.48	8	3.84	209	1.38	0.57	10.45	3.4	202	1.3	627	500.8	79.9
60	20	95	7.5	0.46	8	3.85	209	1.27	0.54	10.4	3	209	1.3	624	497.5	79.7
60	20	100	7.5	0.43	7	4.14	207.5	1.2	0.52	9.47	3.2	207	1.2	568.2	456	80.2

				Simulation Results						Experimental Results						
V_{dc} (V)	C_{ac} (μF)	Load (Ω)	L_{filter} (mH)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	P_{in} (W)	P_{out} (W)	Eff (%)
65	10	75	7.5	0.66	9.5	4.47	213	1.7	0.69	12.25	4.9	210	1.6	796.2	631.8	79.3
65	10	80	7.5	0.65	8	4.44	200	1.56	0.66	10.4	4.8	201	1.4	676	539.7	79.8
65	10	85	7.5	0.65	8	4.4	206.5	1.48	0.66	10.18	4.9	203	1.4	661.7	528.3	79.8
65	10	90	7.5	0.65	8	4.36	213	1.41	0.66	10.13	4.7	206	1.3	658.4	525.3	79.8
65	10	95	7.5	0.63	7	4.6	207	1.34	0.66	10.08	4.6	210	1.3	655.2	522.1	79.7
65	10	100	7.5	0.61	7	4.58	213	1.27	0.66	10.14	4.8	216	1.3	659.1	524.9	79.6
65	20	75	7.5	0.51	8.5	3.53	204	1.63	0.58	12.78	3.6	214	1.6	830.7	669.6	80.6
65	20	80	7.5	0.48	8	3.8	206	1.48	0.57	10.79	3.5	203	1.5	701.3	566	80.7
65	20	85	7.5	0.46	8	3.82	207	1.41	0.54	10.72	3.9	204	1.4	696.8	564.5	81

				Simulation Results						Experimental Results						
V_{dc} (V)	C_{ac} (μF)	Load (Ω)	L_{filter} (mH)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	P_{in} (W)	P_{out} (W)	Eff (%)
65	20	90	7.5	0.43	7	4.1	206	1.34	0.52	9.82	4.1	202	1.4	638.3	515.3	80.7
65	20	95	7.5	0.41	7	4.3	206.5	1.27	0.49	8.9	3.6	205	1.3	578.5	471.9	81.6
65	20	100	7.5	0.39	7	4.8	206	1.2	0.47	8.41	4.2	212	1.2	546.6	443.7	81.2
70	10	75	7.5	0.64	8.5	4.5	209	1.7	0.66	11.31	5.1	212	1.6	791.7	630	79.6
70	10	80	7.5	0.62	7.5	4.7	203	1.56	0.66	11.05	5.1	213	1.5	773.5	619	80
70	10	85	7.5	0.62	7.5	4.65	209.5	1.41	0.65	9.12	5.1	198	1.8	638.4	517.1	81
70	10	90	7.5	0.6	6.5	4.98	202	1.34	0.64	9.11	4.9	203	1.3	637.7	516.3	81
70	10	95	7.5	0.6	6.5	4.97	209	1.45	0.64	9.06	4.9	207	1.3	634.2	512	80.7
70	10	100	7.5	0.59	6.5	4.95	215	1.27	0.63	8.08	5.2	201	1.2	565.6	457.6	80.9

				Simulation Results						Experimental Results						
V_{dc} (V)	C_{ac} (μF)	Load (Ω)	L_{filter} (mH)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	P_{in} (W)	P_{out} (W)	Eff (%)
70	20	75	7.5	0.48	8.5	3.79	211	1.63	0.54	11	3.6	209	1.6	770	631.9	82.1
70	20	80	7.5	0.44	8	3.81	213	1.56	0.52	10.02	4.3	201	1.5	701.4	576.9	82.2
70	20	85	7.5	0.42	7.5	4.08	212	1.48	0.52	10.38	4.3	213	1.5	726.6	595.3	81.9
70	20	90	7.5	0.41	7	4.28	213	1.38	0.47	8.62	3.6	206	1.4	603.4	497.6	82.5
70	20	95	7.5	0.39	6.5	4.79	213	1.34	0.44	8.1	3.7	207	1.3	567	466	82.2
70	20	100	7.5	0.36	6	4.34	208	1.2	0.45	8.26	3.5	213	1.3	578.2	472.8	81.8
75	10	75	7.5	0.62	8	4.74	211	1.7	0.64	10.04	4.7	209	1.6	753	612.8	81.4
75	10	80	7.5	0.6	7	5.05	204	1.56	0.64	9.83	5.1	208	1.5	737.2	600.3	81.5
75	10	85	7.5	0.6	7	5.01	210	1.48	0.63	8.74	4.9	205	1.4	655.5	534.1	81.5

				Simulation Results						Experimental Results						
V_{dc} (V)	C_{ac} (μF)	Load (Ω)	L_{filter} (mH)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	P_{in} (W)	P_{out} (W)	Eff (%)
75	10	90	7.5	0.59	7	4.98	216	1.41	0.61	8.65	5.2	206	1.4	648.7	528.6	81.5
75	10	95	7.5	0.58	6	4.27	203.3	1.27	0.61	8.61	5	210	1.3	645.7	526.6	81.5
75	10	100	7.5	0.58	6	4.27	209.5	1.27	0.59	7.57	5.6	206	1.2	567.7	462.5	81.5
75	20	75	7.5	0.43	7.5	4.04	206	1.63	0.52	10.57	3.8	213	1.6	792.7	658.3	83
75	20	80	7.5	0.41	7	4.25	207	1.56	0.47	8.81	3.8	204	1.5	660.7	549.3	83.1
75	20	85	7.5	0.39	7	4.75	208	1.48	0.44	8.23	3.8	205	1.4	617.2	513.2	83.1
75	20	90	7.5	0.36	6	4.29	204	1.34	0.44	8.45	3.6	213	1.4	633.7	525.2	82.9
75	20	95	7.5	0.33	6	4.49	212	1.31	0.4	7.23	4.3	203	1.3	542.2	449.1	82.8
75	20	100	7.5	0.31	6	5.05	213	1.24	0.37	6.77	4.8	203	1.2	507.7	418.4	82.4

				Simulation Results						Experimental Results						
V_{dc} (V)	C_{ac} (μF)	Load (Ω)	L_{filter} (mH)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	P_{in} (W)	P_{out} (W)	Eff (%)
80	10	75	7.5	0.6	7.5	5.09	211	1.7	0.61	9.51	5.2	208	1.6	760.8	626.1	82.3
80	10	80	7.5	0.58	6	4.28	198	1.48	0.61	9.3	5.4	210	1.5	744	612.7	82.4
80	10	85	7.5	0.58	6.5	4.27	204	1.41	0.59	8.05	5.6	202	1.4	644	530.5	82.4
80	10	90	7.5	0.58	6	4.27	210.5	1.41	0.59	8.05	5.5	208	1.4	644	531	82.4
80	10	95	7.5	0.54	6	4.57	214.5	1.38	0.59	8.07	5.6	205	1.3	645.6	529	81.9
80	10	100	7.5	0.53	5.5	5.12	208	1.27	0.58	6.55	4.8	200	1.2	524	428.3	81.7
80	20	75	7.5	0.4	7	4.23	204	1.66	0.47	9.15	3.8	208	1.7	732	615.2	84
80	20	80	7.5	0.39	7	4.72	212	1.56	0.44	8.6	4.2	207	1.5	688	576	83.7
80	20	85	7.5	0.36	6.5	4.26	208	1.45	0.42	7.88	3.7	209	1.3	630.4	528.1	83.8

				Simulation Results						Experimental Results						
V_{dc} (V)	C_{ac} (μF)	Load (Ω)	L_{filter} (mH)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	D	I_{dc} (A)	THD (%)	VLL_{rms} (V)	I_{rms} (A)	P_{in} (W)	P_{out} (W)	Eff (%)
80	20	90	7.5	0.31	6	5.01	208	1.34	0.4	7.57	3.8	208	1.4	605.6	505	83.4
80	20	95	7.5	0.29	5.5	5.13	208	1.27	0.37	7.1	4.8	207	1.3	568	472	83.1
80	20	100	7.5	0.26	5	5.82	210	1.24	0.35	6.35	4.4	204	1.2	508	419.7	82.6